


Comp 310
Computer Systems and Organization

Lecture #21

I/O Systems

Prof. Joseph Vybihal



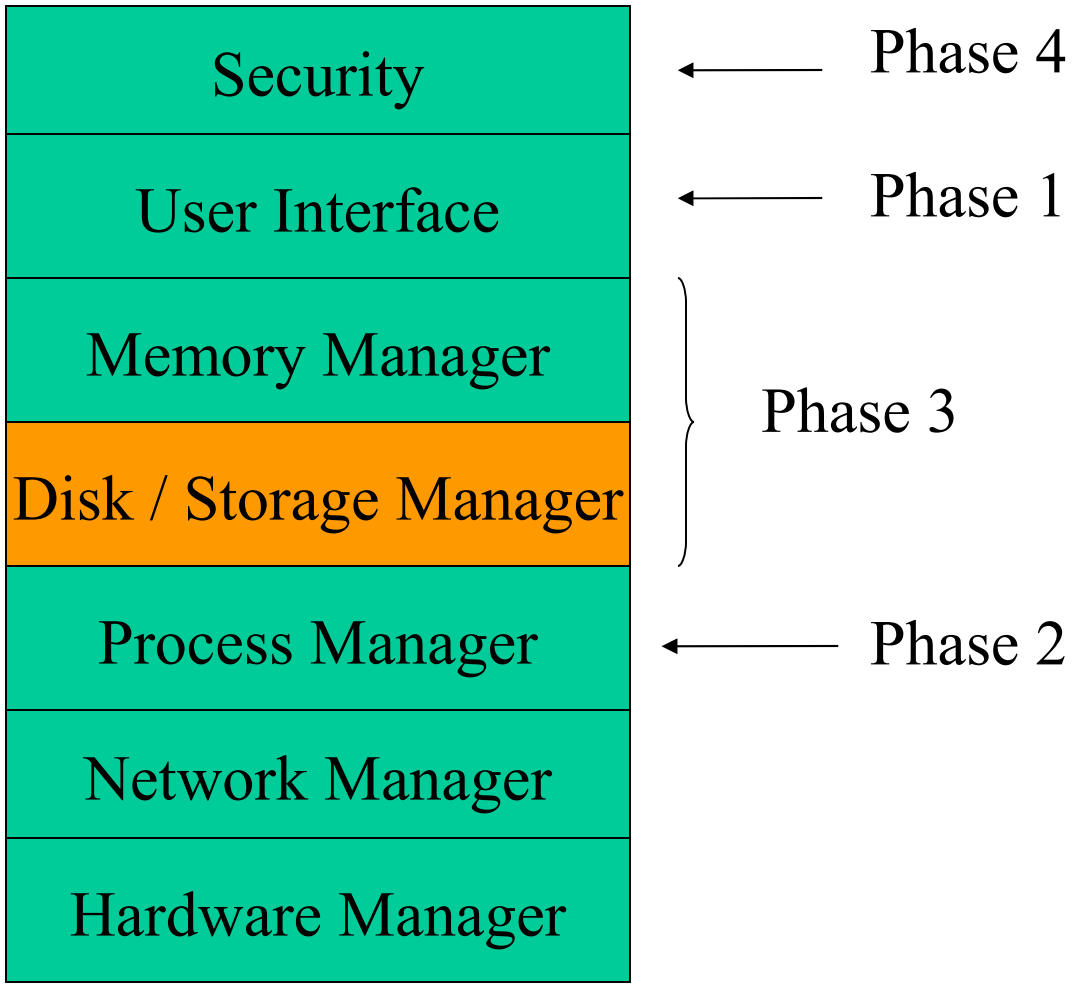

Announcements

- Final Exam Dec 9, 2PM
- **Course Evaluations**




Basic OS Architecture

(Course Table of Contents)





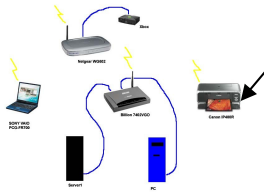

Part 1

I/O Systems

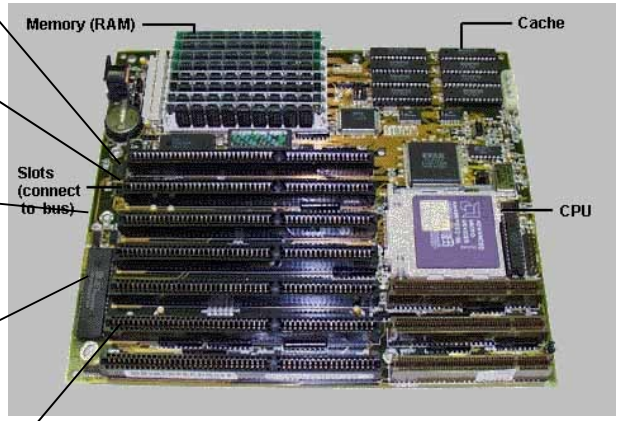
General Purpose OS

A Manager

The OS



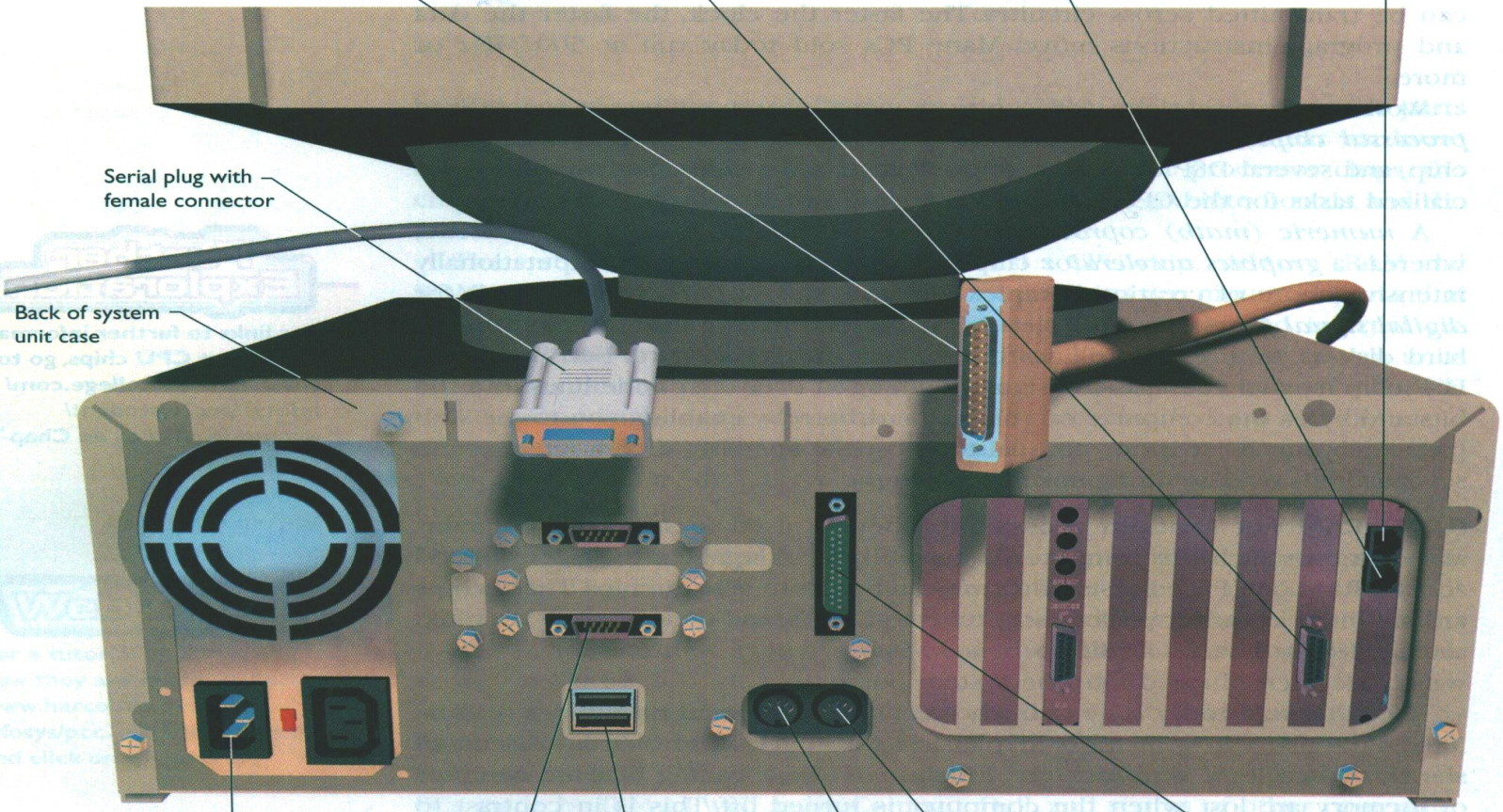
OS manages through the system board



Being a Device Manager is one of the OS's biggest jobs.

Equal to process and memory management.

Computer Ports



MONITOR PORT
The monitor port is used to connect a monitor.

MODEM CONNECTOR
Plug the modem jack in here and connect the other end to the phone outlet.

PHONE CONNECTOR
If you unplugged a telephone to connect your modem, plug the cable from the phone in here.

Parallel plug with male connector

Serial plug with female connector

Back of system unit case

POWER CONNECTOR
The power connector is used with a special cable to connect to a wall outlet.

SERIAL PORT
Serial ports, which have either 9 or 25 pins, are used to connect such low-speed peripherals as scanners and external modems.

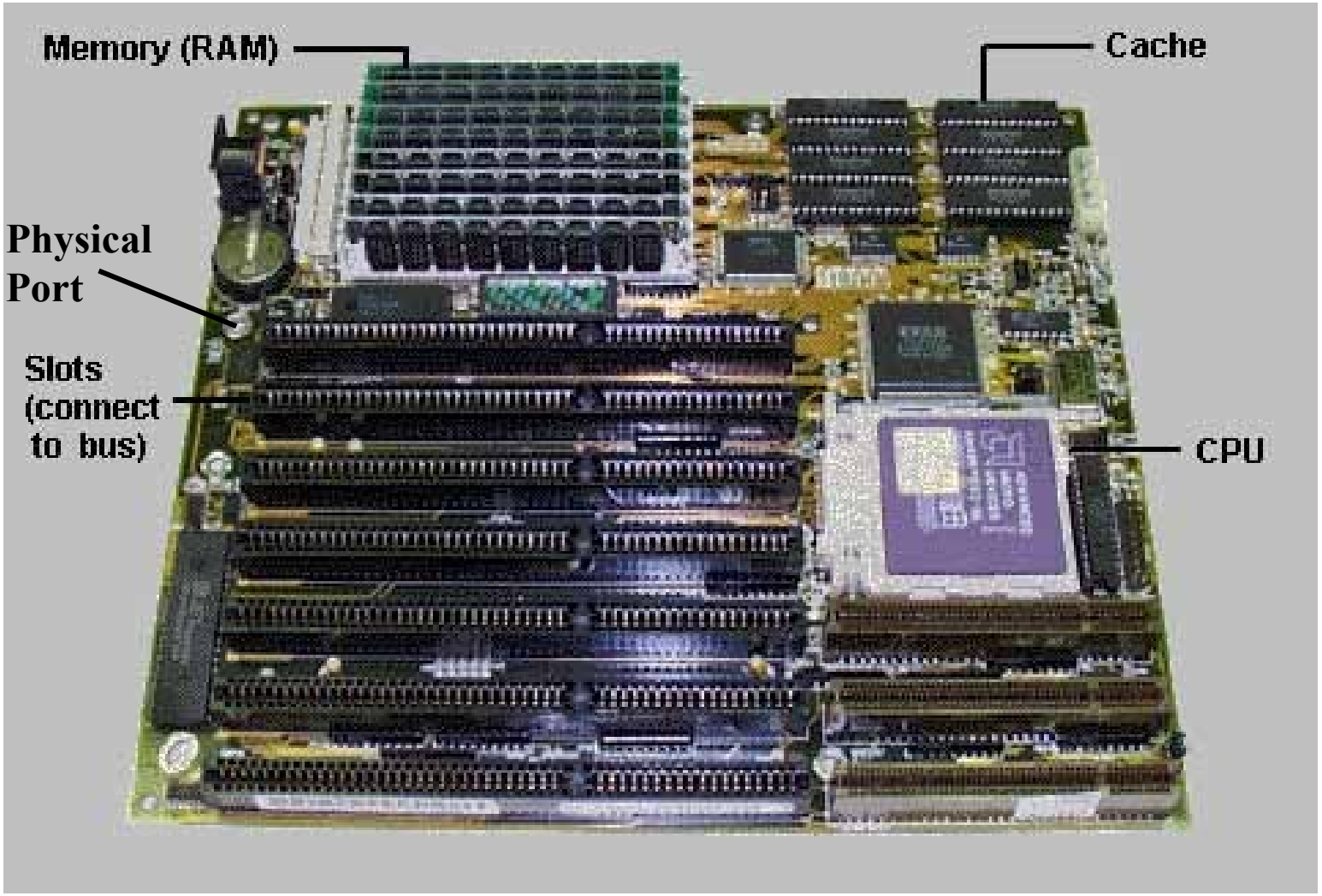
USB PORT
USB ports allow you to connect several devices to a single port. Most new computers come with two USB ports.

MOUSE PORT
The mouse port is used to connect a mouse.

KEYBOARD PORT
The keyboard port is used to connect a keyboard.

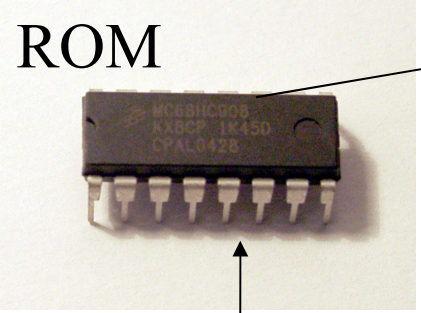
PARALLEL PORT
Parallel ports have 25 holes and are most commonly used for printers and tape drives.

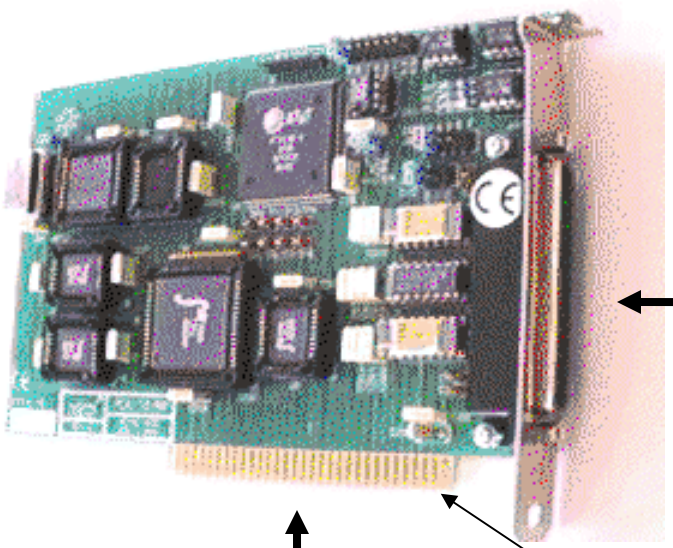
The Motherboard/System Board



Devices connect via Physical Ports or System Slots – **no other way**

Slots, Cards, Ports & ROMS





Printer Port

Each pin is a bit to a register

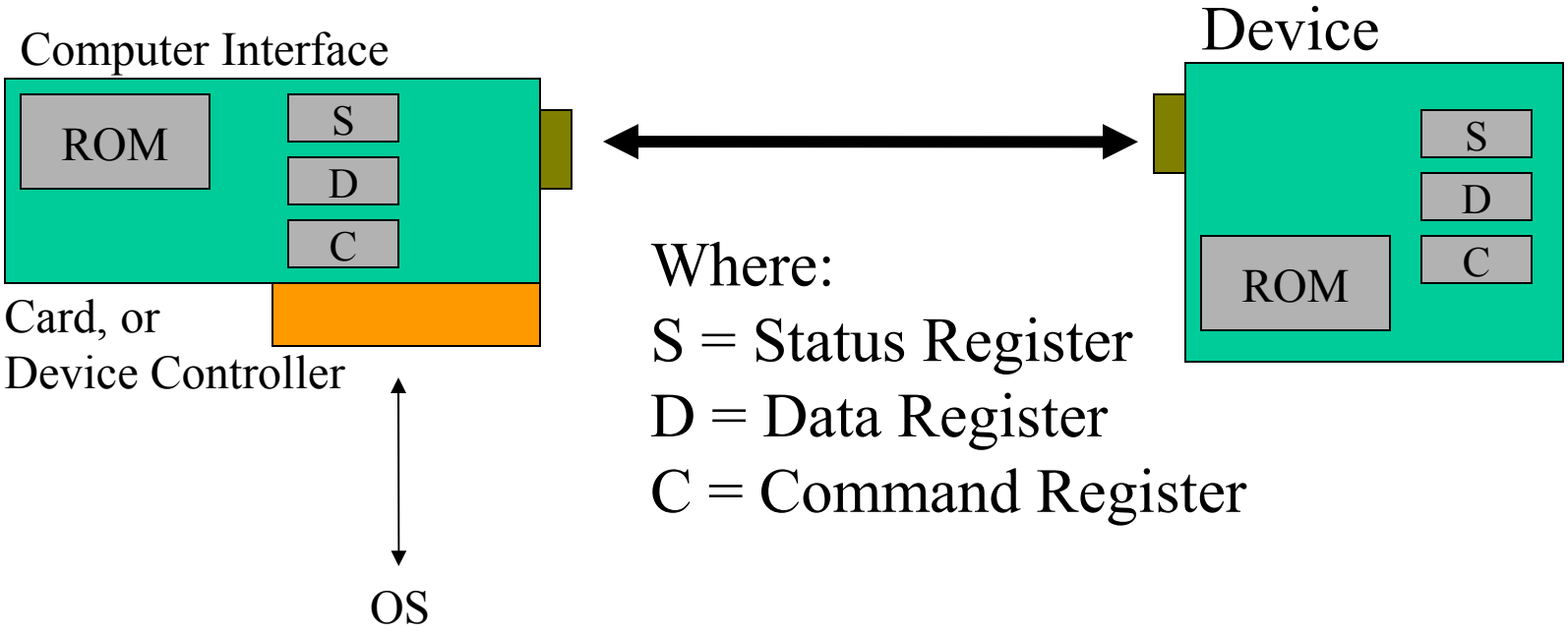
Interconnected

One PIN of data (bit)

OS

A Slot

Flow Diagram



Device Operation:

2. Device updates S (optionally D)

- Waits a small unit of time and then reads C and D
  (possible data loss)

Polling Method:

- Check S for change in a busy loop
- If change then copy S and D to memory

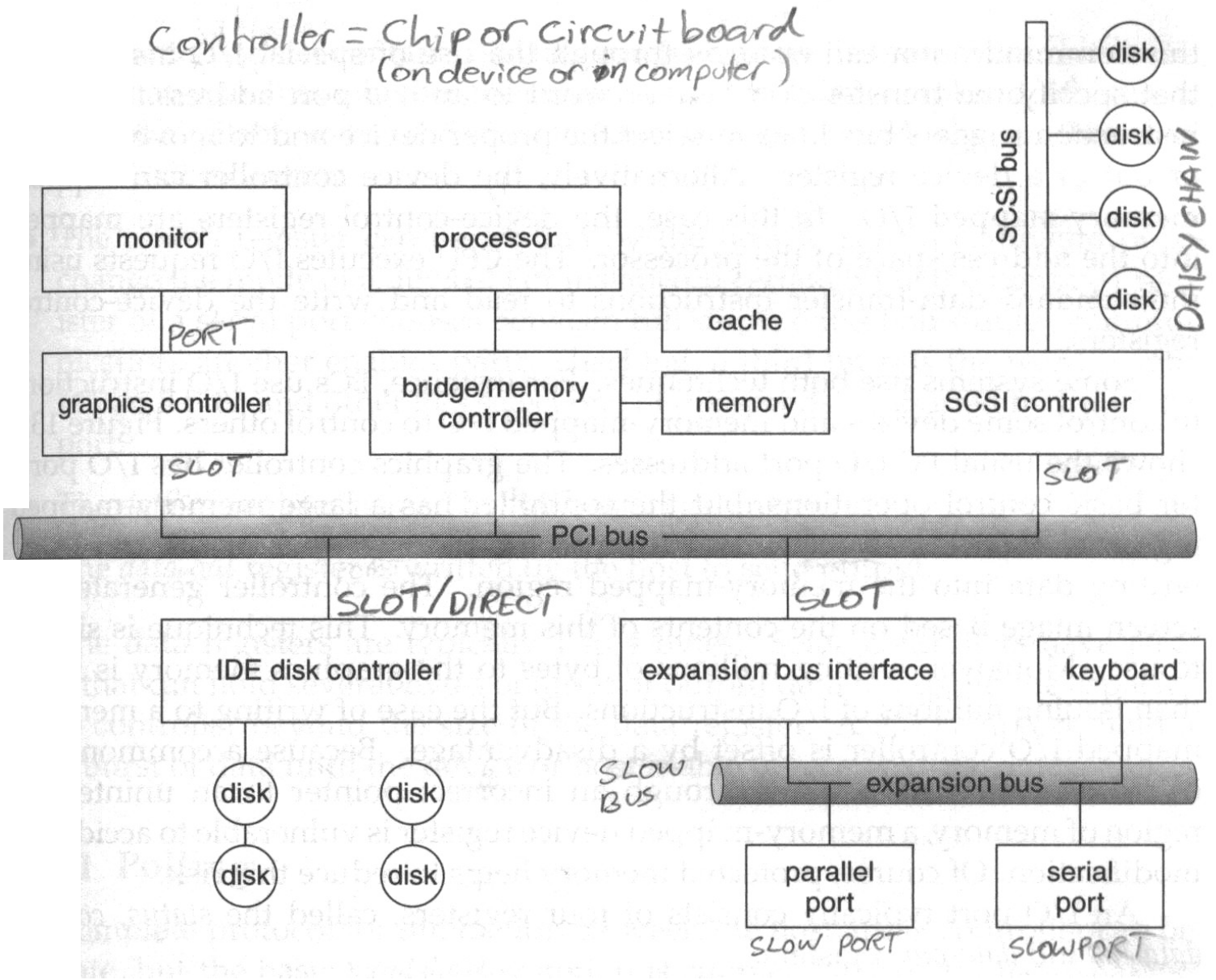
Interrupt Method:

- If S or D updated signal CPU
- CPU Task switch to OS




Question

- Using pseudo-assembler, how would the OS implement polling for a process?
  - How would this relate to the process' ready or sleep queue status?
  - How would the OS manage this:
    - Queue, assembler and interrupts?


Controller = Chip or circuit board
(on device or in computer)
monitor
processor
cache
bridge/memory controller
memory
graphics controller
PORT
SLOT
SCSI bus
disk
disk
disk
disk
DAISY CHAIN
SCSI controller
SLOT
PCI bus
SLOT/DIRECT
SLOT
IDE disk controller
expansion bus interface
keyboard
disk
disk
disk
disk
SLOW BUS
expansion bus
parallel port
SLOW PORT
serial port
SLOWPORT

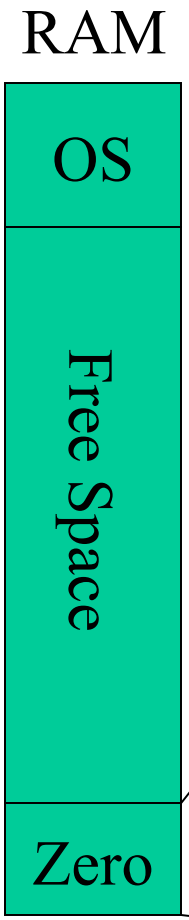



Access to Information

- So… all the information is in those cards and chips… how do I get access to them?

- Direct Memory Mapped I/O
  - A section of RAM wired to system board:
    - Slots, and
    - Physical Ports
  - Any activity that occurs in a slot or port is mirrored in this section of RAM
  - This section of RAM is a two-way path (Input and Output) to these slots and ports
- Direct Memory Access
  - The device can write directory to RAM without the OS or CPU

Memory Mapped I/O



RAM MAP TO

I/O address range (hexadecimal)	device
000-00F	DMA controller
020-021	interrupt controller
040-043	timer
200-20F	game controller
2F8-2FF	serial port (secondary)
320-32F	hard-disk controller
378-37F	parallel port
3D0-3DF	graphics controller
3F0-3F7	diskette-drive controller
3F8-3FF	serial port (primary)

Partial IBM PC Mapped Address Space




Assembler/Pointer Programming

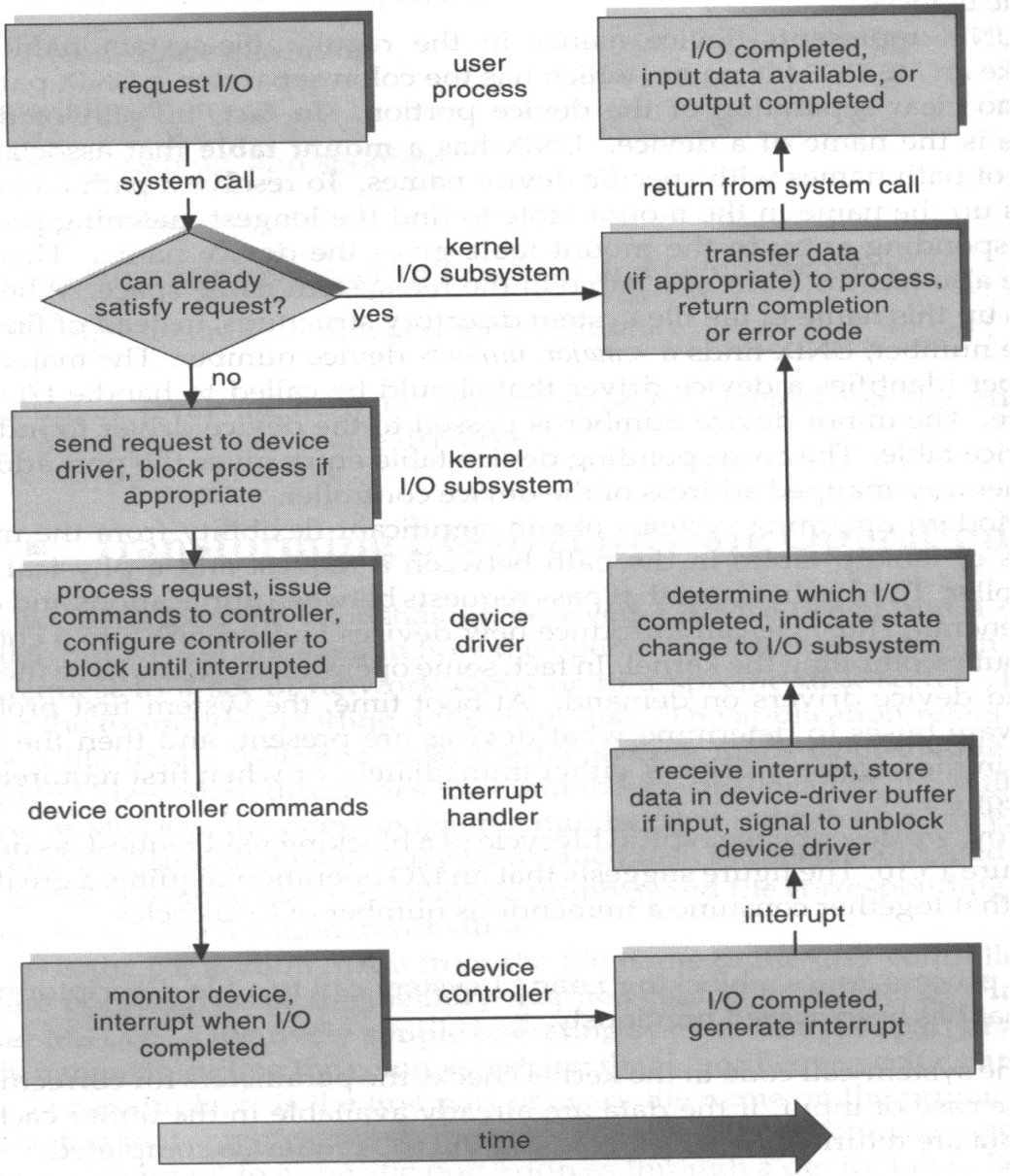
- To take advantage of this memory mapped space requires low-level programming.
- Two low-level programming techniques are used:
  - Polling, and
  - Interrupts



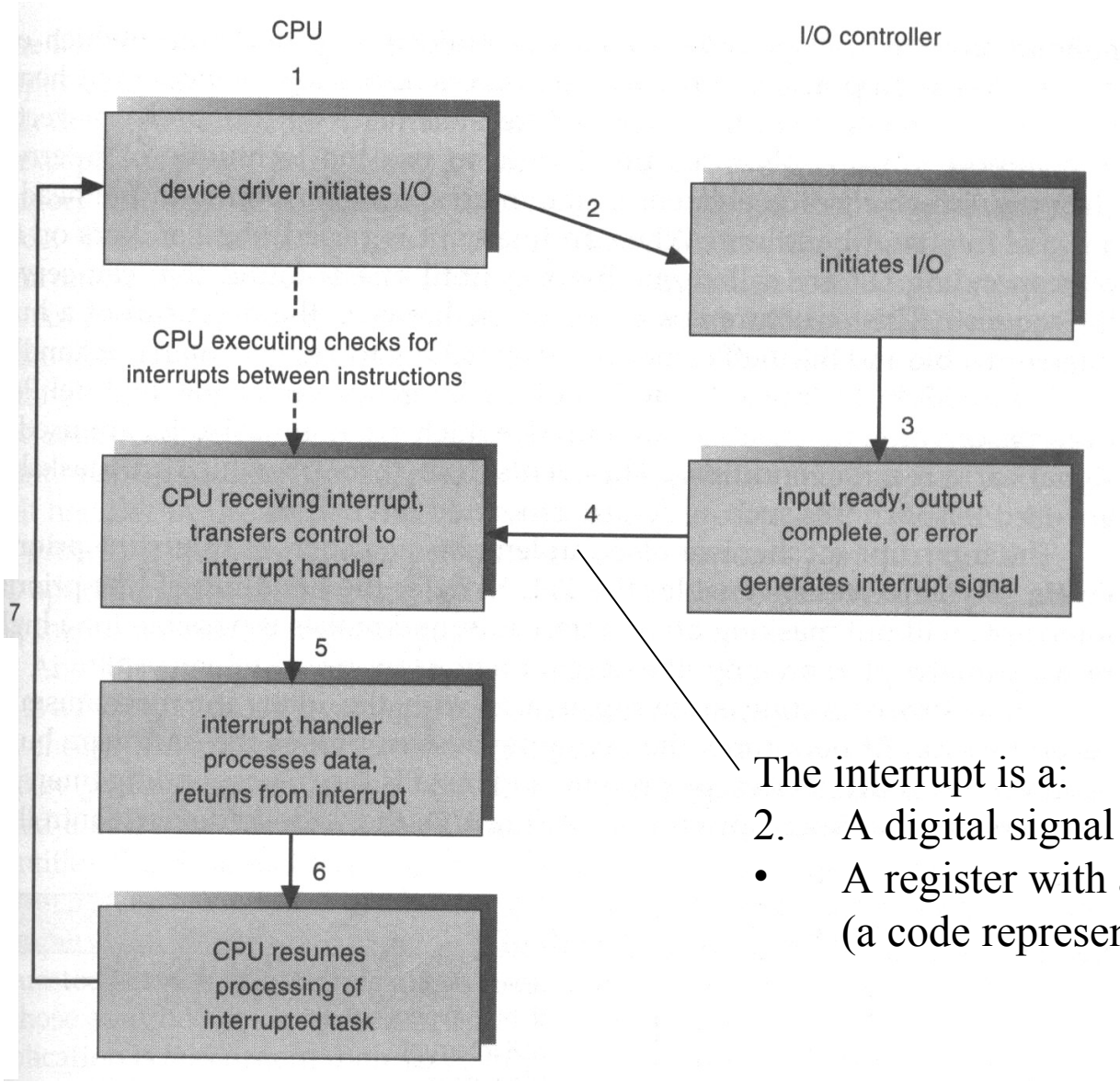

Polling

- Handshaking
  - OS waits for device to indicate that it is not busy
  - OS then deposits a command and data to device registers
  - Device now performs action & OS waits
  - Device returns status information
  - OS reads this information
- Waiting
  - Is a while-loop (a busy loop) that does nothing but loop until the wait is over
  - The OS knows when the wait is over because the device updates the Status register to indicate its state.
- Simple mechanism inserted directly into any OS fn

Hardware Communication



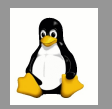
The Interrupt Process



The interrupt is a:

2. A digital signal to stop the CPU
- A register with an integer number (a code representing a message)





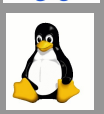

Sample INTEL Interrupt Codes

Note: not dependent on OS, but CPU & Device

vector number	description
0	divide error
1	debug exception
2	null interrupt
3	breakpoint
4	INTO-detected overflow
5	bound range exception
6	invalid opcode
7	device not available
8	double fault
9	coprocessor segment overrun (reserved)
10	invalid task state segment
11	segment not present
12	stack fault
13	general protection
14	page fault
15	(Intel reserved, do not use)
16	floating-point error
17	alignment check
18	machine check
19–31	(Intel reserved, do not use)
32–255	maskable interrupts

INTEL Pentium Processor event-vector

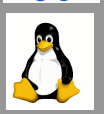





Interrupt Handling

- Interrupt Handler
  - A special function called to process an interrupt from a specific device
  - Each device needs a custom handler
  - The handler is aware of the registers and codes used by that specific device (this is true for polling as well)
- Interrupt Messages
  - Stored as codes in registers
  - Two code types:
    - Integers (integer code number representing a message)
      - Processed by a switch statement
    - Flags (a bit set to 1 for true or 0 for false)
      - Processed by bit masking



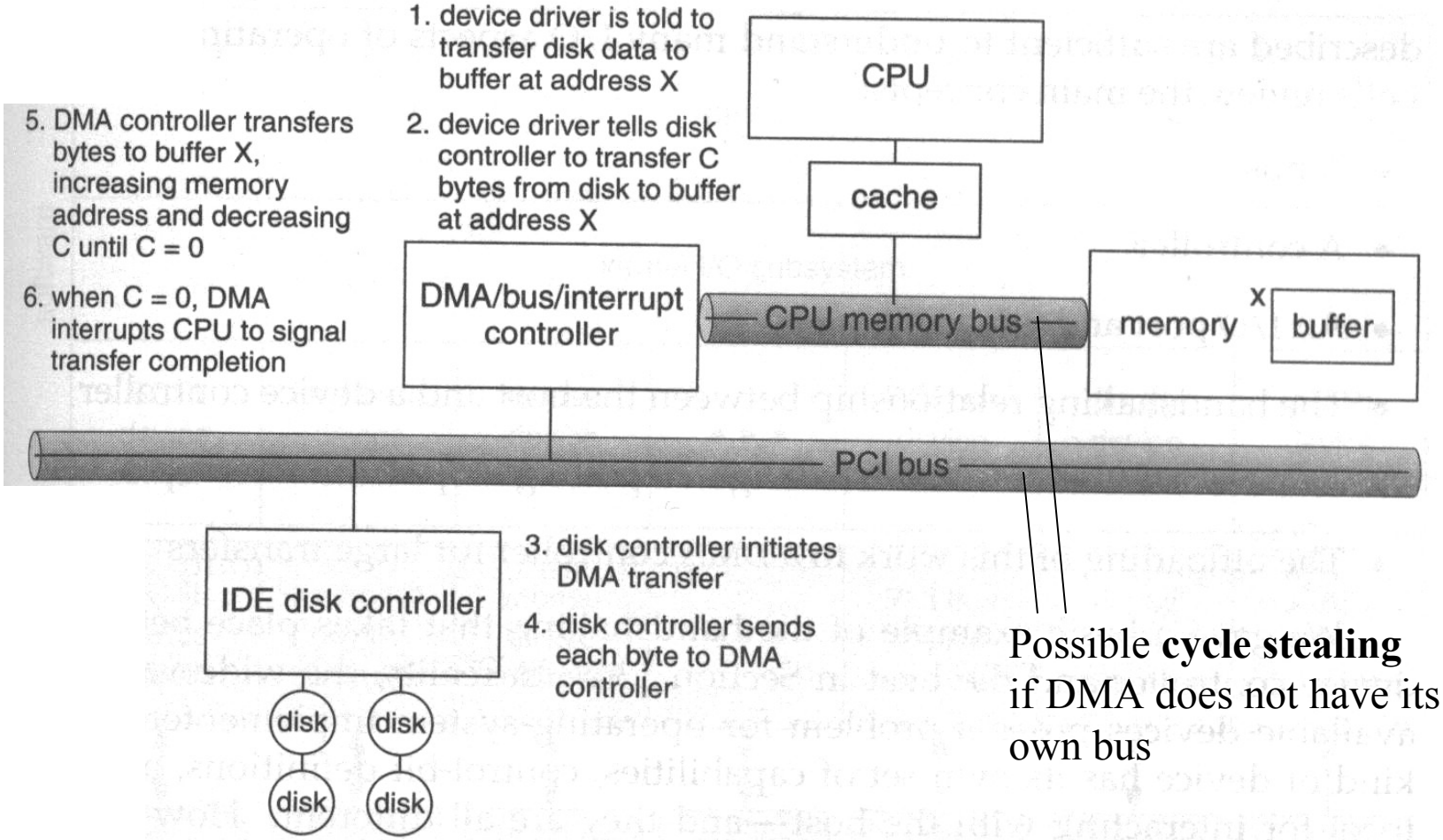



Interrupt Notes

- Software can also issue interrupts
  - Timers
  - Java Action Listeners
- Interrupts can be interpreted by the OS as having priority
  - Ordering how the OS will process them
    - User interface interrupts have higher priority
- Interrupts that are not handled quickly by the OS can be overwritten by the next hardware signal
- Each CPU and device has their own event-vector table with their own unique codes
  - Microsoft Mouse
  - Logitech Mouse

MDA

(Direct Memory Addressing)



Possible **cycle stealing** if DMA does not have its own bus




Part 2

The OS Point-of-view

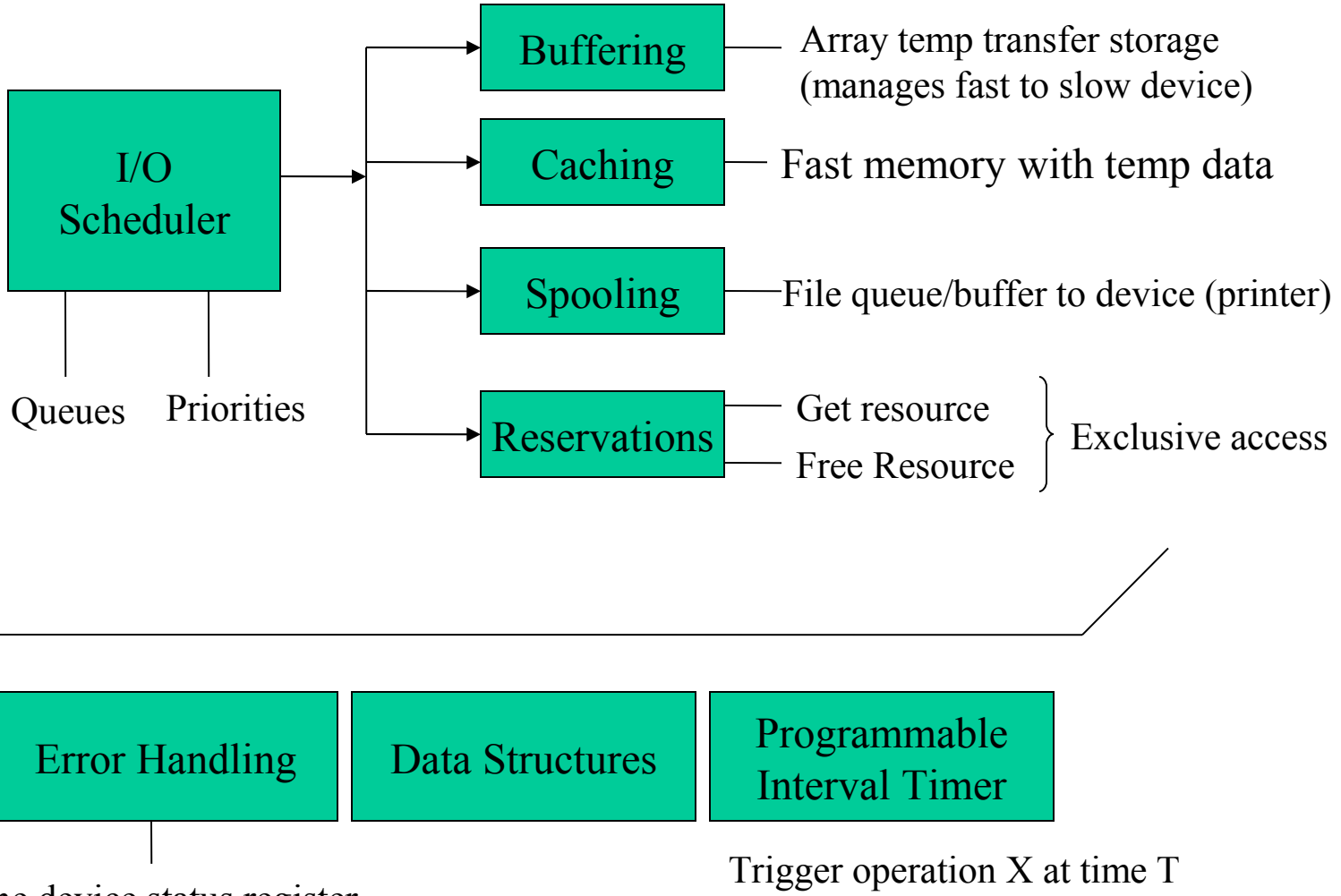



Management Issues

- Device hardware specifications
- Device communication features
- Motherboard data transfer features
- Optimization & Impact on Process
  - Speed
  - Memory
- Security

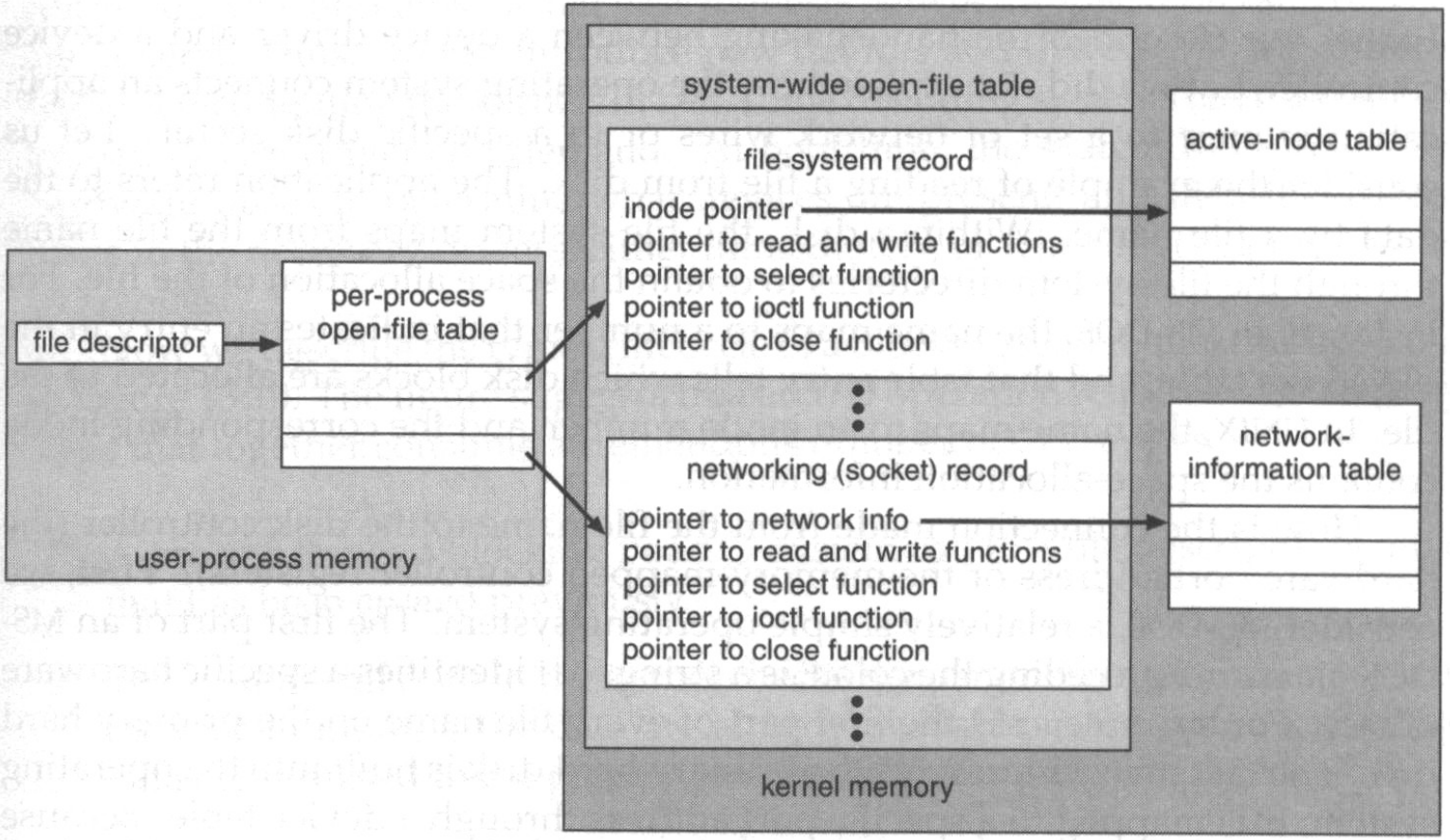



I/O Sub-System Architecture



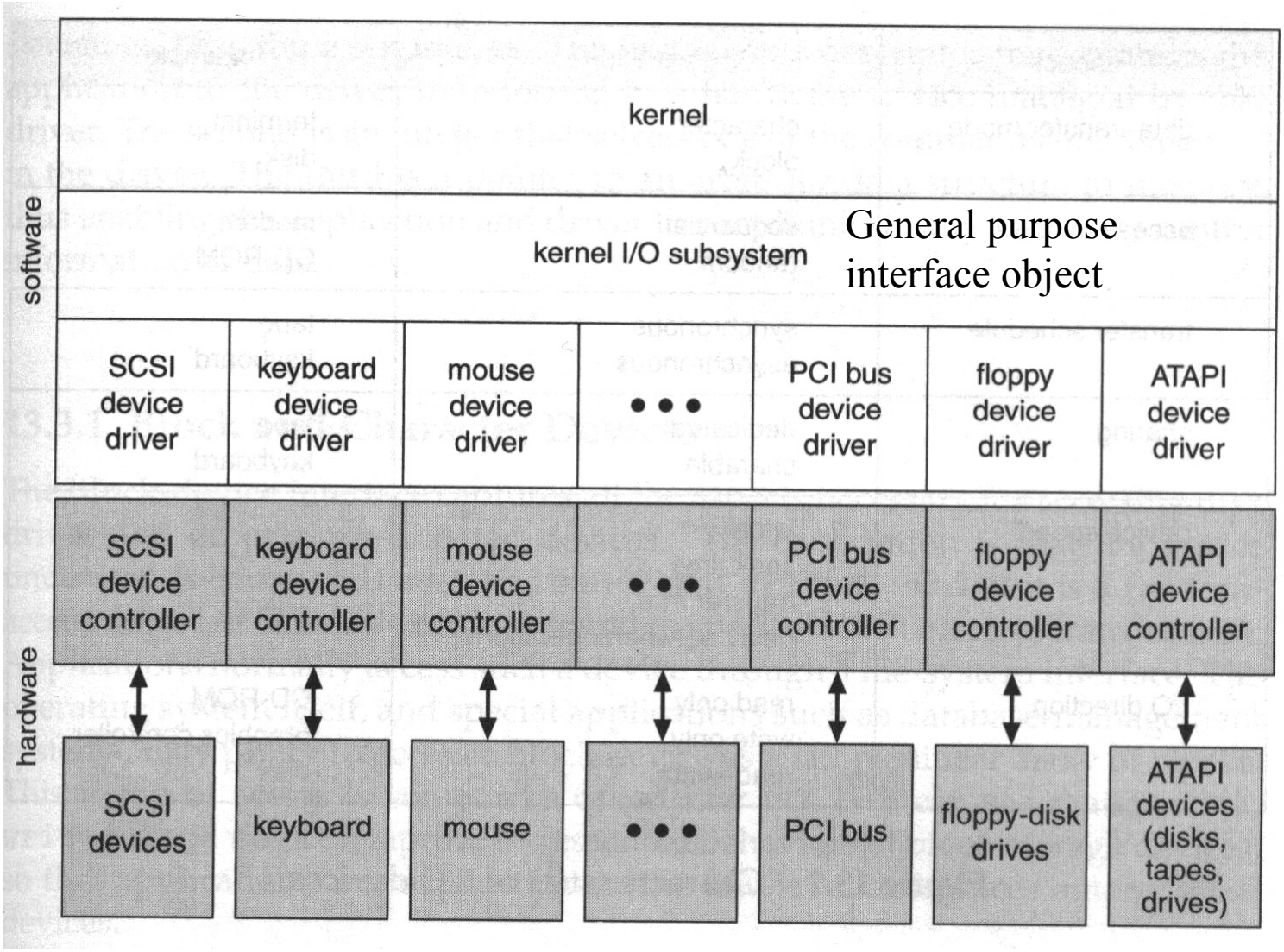
UNIX I/O Kernel Data Structure

(Example – partial structure)



Only shows file I/O

The Kernel I/O Structure



Multiple specific drivers




Device Communication Features

Each device speaks differently

aspect	variation	example
data-transfer mode	character block	terminal disk
access method	sequential random	modem CD-ROM
transfer schedule	synchronous asynchronous	tape keyboard
sharing	dedicated sharable	tape keyboard
device speed	latency seek time transfer rate delay between operations	
I/O direction	read only write only read–write	CD-ROM graphics controller disk




Device Communication Modes

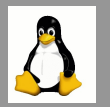
- Block Driven
  - I/O cannot function by byte
  - I/O access by a fixed number of bytes called a block
  - The entire set of bytes is loaded into a buffer as a single unit
- Character Stream
  - I/O access is by byte
  - A pointer increments past each byte
- Socket Based
  - An object that references a specific physical port
  - The user's application has a reference to this object
  - The object manages communication with the device



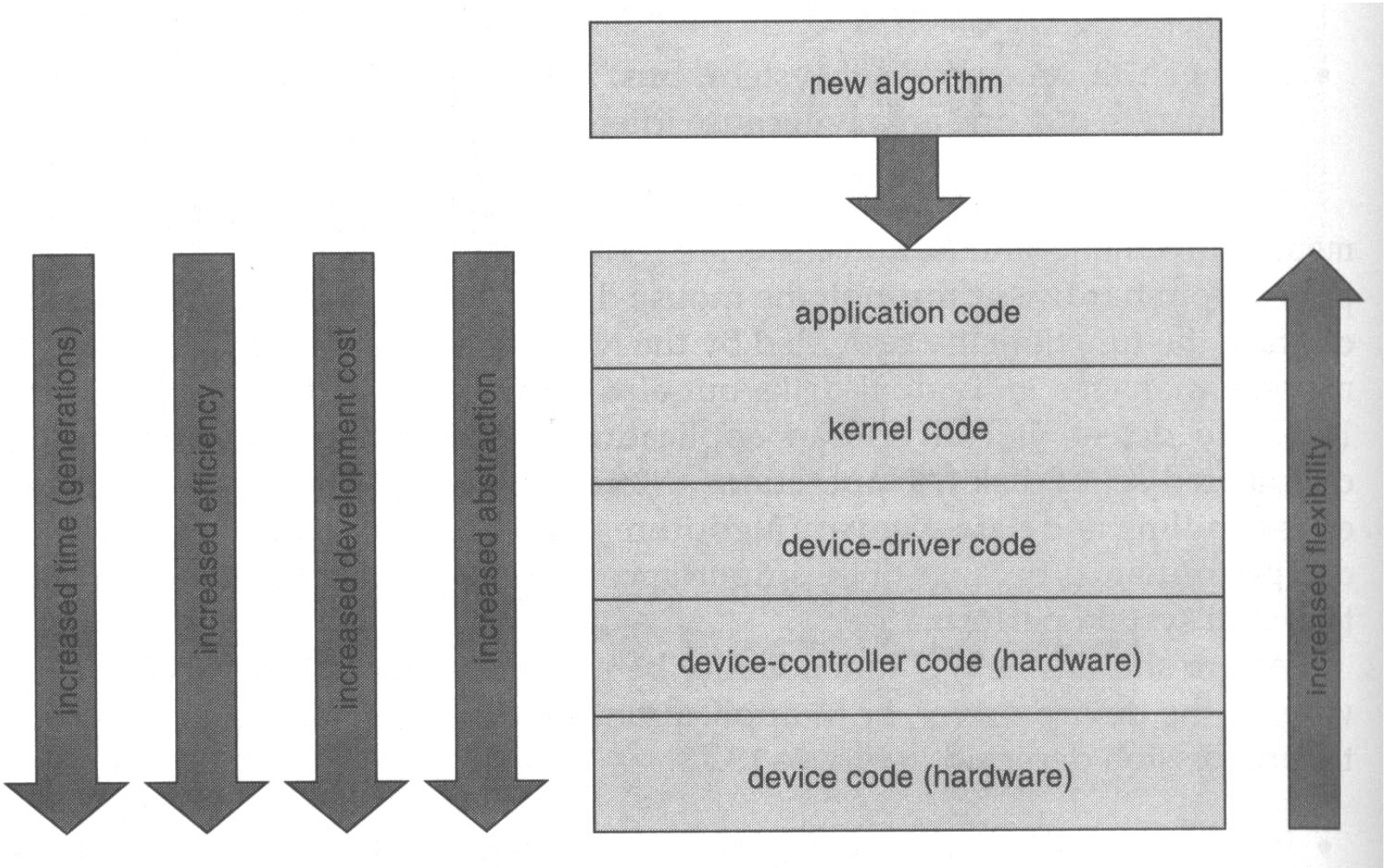

Device Communication Modes

- Blocking I/O
  - Stop executing process
  - Switch to driver
- Non-Blocking I/O
  - Device data accesses as a running process
    - Keyboard
    - Mouse






Programming Complexity






Part 3

At Home




Things to try out

1. Have you every installed a driver?
2. Web Resources (I/O Systems):
   - http://www.cs.mun.ca/~paul/cs3725/material/web/notes/node28.html
   - http://download.oracle.com/docs/cd/B19306_01/server.102/b14211/iodesign.htm
   - http://www.freebsd.org/doc/en_US.ISO8859-1/books/design-44bsd/overview-io-system.html