Midterm Examination # 1

Electronic Circuits I - ECSE-330B
February 14th 2008, 8:35 AM – 9:55 AM
Professor Ramesh Abhari

Pertinent Information:

1) This is a closed-book examination, no notes permitted.

2) This examination consists of 4 questions with total possible points of 50. Partial point distribution is indicated in brackets.

3) Only the Faculty Standard Calculator is permitted.

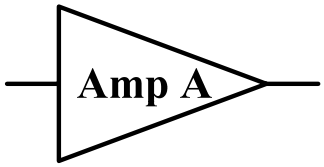
4) Show your work: answers without justification will not receive marks. State any assumption you find necessary to complete your answer.

Last Name	
First Name	
Student Number	

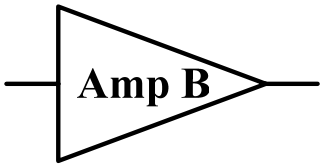
Question	Mark
1	/15
2	/15
3	/10
4	/10
Total	/50

QUESTION 1 *(15 marks)*

(a) What is the best way to connect two voltage amplifiers shown below between a 10 KΩ source and a 100Ω load in order to achieve maximum voltage gain? (2 marks)



Input resistance = 2K Ω
Output resistance = 100 Ω
Open circuit voltage gain = 50



Input resistance = 100K Ω
Output resistance = 1K Ω
Open circuit voltage gain = 100

(b) Find an expression for the overall voltage gain of the system based on your choice in part (a) and calculate its value. (6 marks)

(c) The circuit in part (a) is now modified by connecting a 5nF decoupling capacitor at the input of the first stage and a 1nF capacitor in parallel with the load:

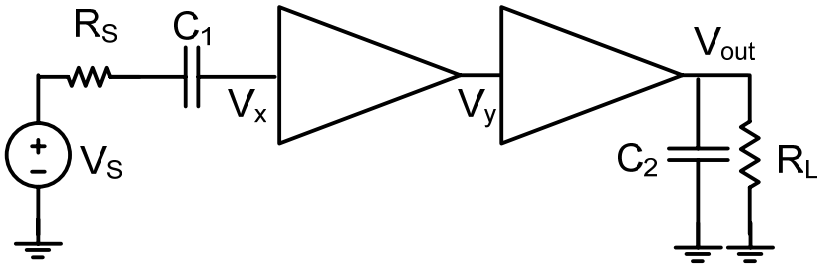


Figure 1

I) Find the 3-dB frequency associated with C_1 (Hint: one way to find this frequency is from the transfer function V_x/V_s). (2 marks)

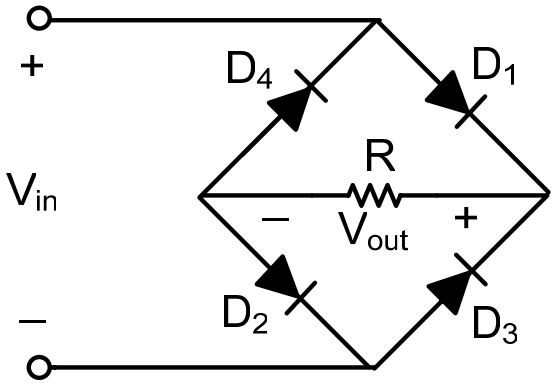
II) Find the 3-dB frequency associated with C_2 (Hint: one way to find this frequency is from the transfer function V_{out}/V_y). (2 marks)

III) Does the amplifier in Figure 1 have lowpass, highpass, bandpass, or bandstop characteristics? (1 mark)

IV) Draw the bode magnitude plot of (V_{out}/V_S) for the amplifier in Figure 1. Clearly label all values. (2 marks)

QUESTION 2 *(15 marks)*

Consider the following rectifier circuit:



Assume that all diodes are identical with n=2 and that R= 4KΩ. Use constant voltage drop (CVD) model for the diodes with $V_{BE}(on)$=0.7V and:

(a) Determine the state of the diodes and find the value of V_{out} for V_{in}= 10V. (4 marks)
(b) Determine the state of the diodes and find the value of V_{out} for V_{in}= -10V. (4 marks)
(c) Draw the voltage transfer characteristics of the rectifier (V_{out} versus V_{in}). Clearly indicate the slope of the lines and transition points. (3 marks)
(d) Assume $V_{in}=V_{in(dc)}+V_{in(ac)}$=10V+1mVcos(10t). Draw the small-signal equivalent circuit and find the small signal voltage gain ($V_{out(ac)}/V_{in(ac)}$). (4 marks)

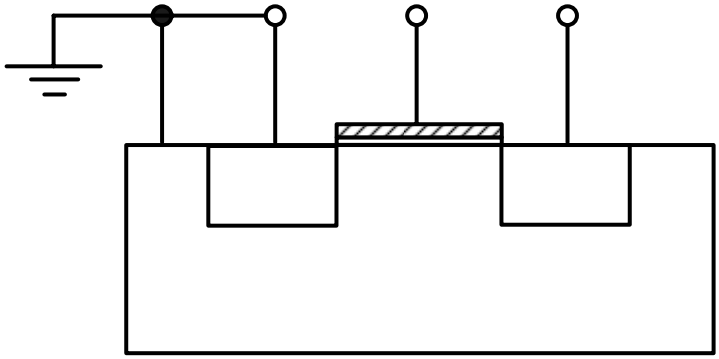
QUESTION 3 *(10 marks)*

(a) Explain the physics behind formation of the depletion region in a PN junction (3 marks). Also explain what happens to the depletion region as the PN junction is:

(i) Reverse biased. (1 mark)
(ii) Forward biased. (1 mark)

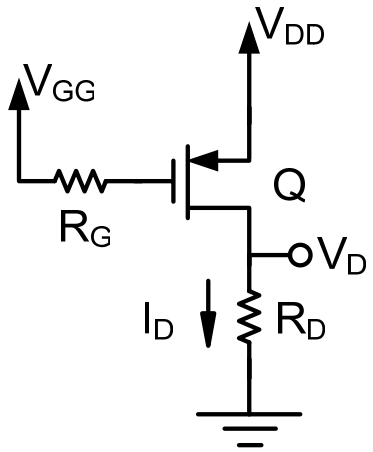
(b) Clearly label Gate, Source, and Drain on the NMOS layout shown below. Also specify the type of doping in each region. (2 marks)

What is channel inversion and how does it happen in NMOS transistors. (3 marks)



QUESTION 4 *(10 marks)*

For the following circuit assume that V_{DD} = 5 V, V_{GG} = 3 V, R_G = 4 KΩ, R_D = 2 KΩ, $\mu_p C_{OX}$ = 100 μA/V^2, $|V_{tp}|$= 1 V, $|\lambda|$= 0.025 V^{-1}and (W/L) = 20.



Include the effect of channel length modulation (CLM) and find:

(a) I_D.

(b) V_D.