McGill

Introduction to SPICE

ECSE 330 Introduction to Electronics

Department of Electrical and Computer Engineering
McGill University

SPICE

- **SPICE** (**S**imulation **P**rogram with **I**ntegrated **C**ircuits **E**mphasis!):
  - Circuit simulation program.
  - Provides detailed analysis of circuits containing lumped components (R, L, C) and active components (diodes, FETs, BJTs).

- PC Version:
  - Pspice A/D (part of Orcad 10.0)
  - Available on the machines on the 4th and 5th floor of the Trottier.
  - You can download PSPICE 9.1 (student edition) it from the following link at your own risk:

    http://electronics-lab.com/downloads/schematic/013/

- Resources:
  - "Spice for Microelectronics" by Roberts and Sedra, 2nd edition.
  - Interactive User Guide from http://bwrc.eecs.berkeley.edu/Classes/IcBook/SPICE

PSpice A/D

- Models the behavior of a circuit containing any mix of analog and digital devices.

- Basic analyses:
  - DC analysis: DC sweep, bias point, DC sensitivity, small-signal DC gain, and input and output resistances.
  - AC analysis: small-signal response over a range of frequencies and noise.
  - Transient analysis: time-domain response and Fourier analysis.

Spice Input File (Deck)

- **Suggested input format:**

Title Statement	*Title statement is always on the first line.*
****Comment	*Comment always begins with an asterisk (*).*
Circuit Description Power Supplies / Sources Element Description Model Statements	*Elements must be uniquely labeled (up to 8 characters, 1st character identifies the type of the element). Connections are represented by nodes, which are usually numbered. Node "0" means ground.*
Analysis Requests	
Output Requests	
.END	*The last line must end with an .END.*

- Additional Notes:
  - Order is not important, except the first and last lines.
  - NOT case sensitive.
  - Words can be separated by an arbitrary number of spaces.

Input File Example

Title → Low pass filter

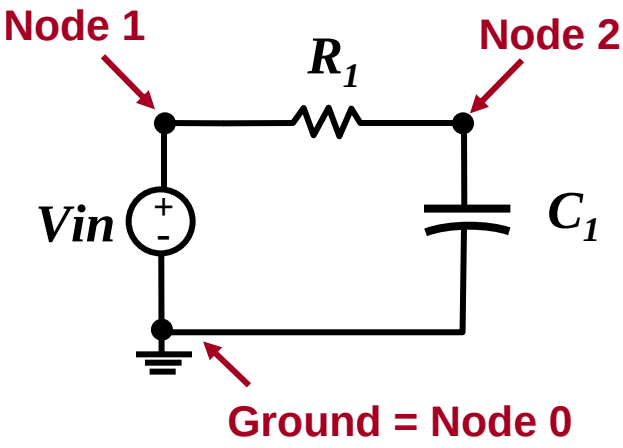
```
** Circuit Description **
* Power supply
Vin 1 0 PWL(0s, 0V,1ms,0V,
+ 1.0001ms, 1V)

* Elements description
R1   1   2 1Kohm
C1   2   0 1uF

*Analysis request
.OP
.Tran 0.1ms 5ms

.end
```

The "+" sign means that the previous command is continued on this line.

Positive Terminal (n+)

Negative Terminal (n-)

.END command



Basic Element Types in Spice

1st Letter Presentation	Element
B	GaAs field-effect transistor (MESFET)
C	Capacitor
D	Diode
E	Voltage-controlled voltage source (VCVS)
F	Current-controlled current source (CCCS)
G	Voltage-controlled current source (VCCS)
H	Current-controlled voltage source (CCVS)
I	Independent current source
J	Junction field-effect transistor (JFET)
K	Coupled inductors
L	Inductor
M	MOS field-effect transistor (MOSFET)
Q	Bipolar transistor (BJT)
R	Resistor
V	Independent voltage source

Scale-factor Abbreviations in Spice

Power-of-Ten Suffix Letter	Metric Prefix	Multiplying Factor
T	tera	10^{12}
G	giga	10^{9}
Meg	mega	10^{6}
K	kilo	10^{3}
M	mili	10^{-3}
U	micro	10^{-6}
N	nano	10^{-9}
P	pico	10^{-12}
F	femto	10^{-15}

Element Dimensions

Spice Suffix	Units
V	Volts
A	Amps
Hz	Hertz
Ohm	Ohm
H	Henry
F	Farad
Degree	Degree
S	Seconds

Circuit Elements – Two Terminal

- **Resistor**

R*name* n+ n- *value*

- **Capacitor**

C*name* n+ n- *value* [IC = *initial_voltage_condition*]

- **Inductor**

L*name* n+ n- *value* [IC = *initial_current_condition*]

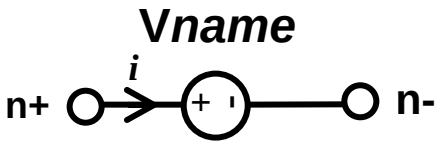
- **Diode**

D*name* n+ n- *dmodel*

.model dmodel D (I_s=1nA n=1)

Independent Sources

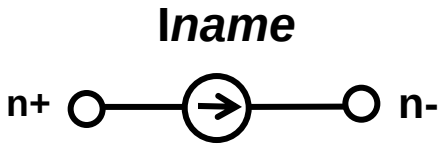
Voltage source:



Current flowing into (n+) is positive

Spice Description	Type of Analysis
V*name* n+ n- DC *value*	All types
V*name* n+ n- AC *Magnitude Phase_deg*	AC Frequency Response
V*name* n+ n- SIN (V_o V_a *freq* t_d *damp*)	Transient
V*name* n+ n- PULSE (V_1 V_2 t_d t_r *PW T*)	Transient
V*name* n+ n- PWL (t_1,v_1 t_2,v_2 … t_n,v_n)	Transient

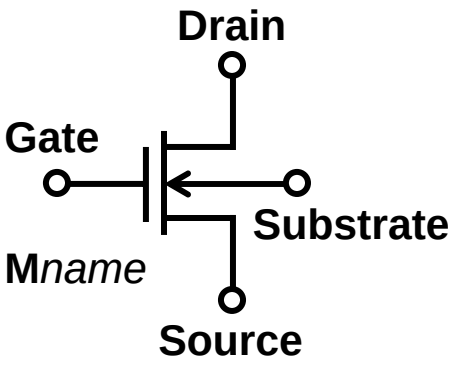
Current source:



The Spice description for an independent current source is the same as the voltage source, except replace “V” by “I”.

Field-Effect Transistors (FETs)

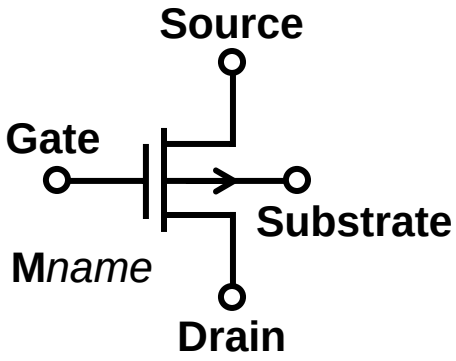
NMOS



Spice description:
M*name* drain gate source substrate *MOS_model_name* L=*value* W=*value*
. MODEL *MOS_model_name* **NMOS** (*parameter_name=value …*)

Example:
M1 2 0 3 3 nmos_enhancement_mosfet L=10u W=400u
.model nmos_enhancement_mosfet nmos (kp=20u Vto=2V lamda=0)

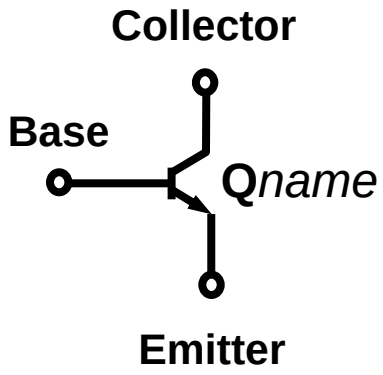
PMOS



Spice description:
M*name* drain gate source substrate *MOS_model_name* L=*value* W=*value*
. MODEL *MOS_model_name* **PMOS** (*parameter_name=value …*)

Bipolar Junction Transistors (BJTs)

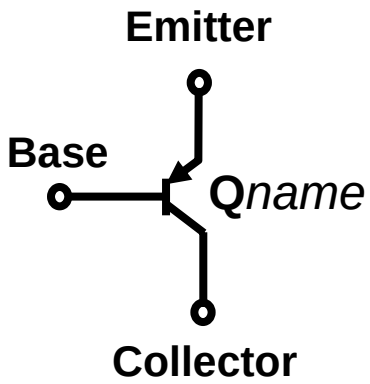
NPN Transistor



Spice description:
Q*name* collector base emitter [substrate] *BJT_model_name* [*#_in_parallel*]
. MODEL *BJT_model_name* **NPN** (*parameter_name=value …*)

Example:
Q1 2 0 3 npn_transistor
.model npn_transistor npn (Is=1.8104e-15 Bf=100)

PNP Transistor



Spice description:
Q*name* collector base emitter [substrate] *BJT_model_name* [*#_in_parallel*]

. MODEL *BJT_model_name* **PNP** (*parameter_name=value …*)

Subcircuit

- Some circuit elements are not always available in the Spice library, *e.g.*, op-amps. To add an op-amp to the Spice deck, a "subcircuit" that represents this op-amp can be defined and incorporated into the main circuit.

- The definition in SPICE for a subcircuit is as follows:

  .SUBCKT *subcircuit_name* list_of_nodes

  Circuit Description

  .ENDS

- To incorporate the subcircuit into the main design, use the following statement, which starts with the letter "X":

  X*name* node_connections *subcircuit_name*

Analysis Requests

Analysis Requests: specify the types of simulations to be performed.

Analysis Requests	**Spice Command**
Operating point	**.**OP
(Calculates DC node voltages and DC currents through voltage sources.)	
Transfer Function	.TF
(Calculates small-signal gain from input to output, input resistance, and output resistance.)	
DC sweep	**.**DC [*type*] *variable start_value stop_value step_value*
AC frequency response	**.**AC DEC *points_per_decade freq_start freq_stop* **.**AC OCT *points_per_octave freq_start freq_stop* **.**AC LIN *total_points freq_start freq_stop*
Transient response	**.**TRAN *time_step time_stop [(no_print_time Max_step_size)]*

DC Sweep

- **Syntax:** .DC [*type*] *variable start_value stop_value step_value*
- *Variable* can be a source name, a model parameter or temperature.
- DC operating point is calculated for each sweep.
- Sweep types:
  - LIN (linear sweep – default)
  - OCT (octave sweep)
  - DEC (sweep by decade)
  - LIST (list of values)
- Examples:
  - .DC Vin -1.2 1.2 0.2
    - Linearly sweeps Vin from -1.2V to +1.2V in 0.2V steps.
  - .DC DEC Ibias 1u 5m 5
    - Sweeps Ibias from 1uA to 5mA using 5 points/decade.

Output Requests

Output Requests: specify the outputs to be displayed.

Analysis Requests	**Spice Command**
Print data points (tabulated data)	**.**PRINT DC *output_variables* **.**PRINT AC *output_variables* **.**PRINT TRAN *output_variables*
Plot data points (tabulated data)	**.**Plot DC *output_variables [(lower_plot_limit upper_plot_limit])* **.**Plot AC *output_variables [(lower_plot_limit upper_plot_limit])* **.**Plot TRAN *output_variables [(lower_plot_limit upper_plot_limit])*
Output Processing	.Probe (saves simulated results for post-processing and plots)

Notes:

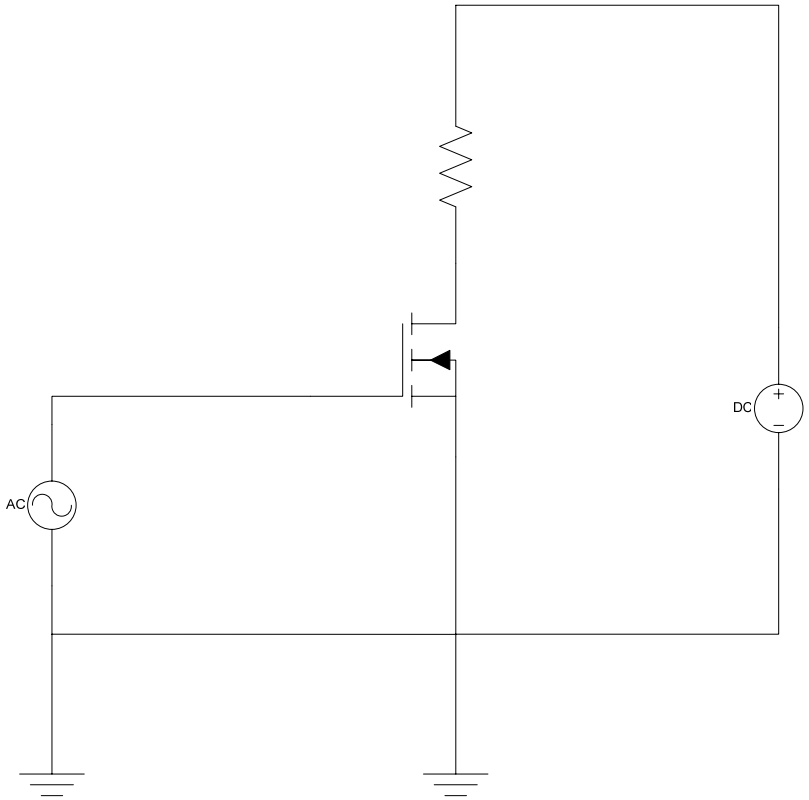
1) Spice *output_variables* can be a voltage at any node V(*node*), the voltage between two nodes V(*node1*,*node2*), or the current through a voltage source I(V*name*).
2) AC *output_variables* can also be
   Vr, Ir: real part
   Vi, Ii: imaginary part
   Vm, Im: magnitude
   Vp, Ip: phase
   Vdb, Idb: decibels

Spice Implementation

- Steps to Identify your circuit:
  - Identify circuit elements
  - Identify node names
  - Write the netlist
    - Use appropriate models.
    - Specify the simulation type you want.

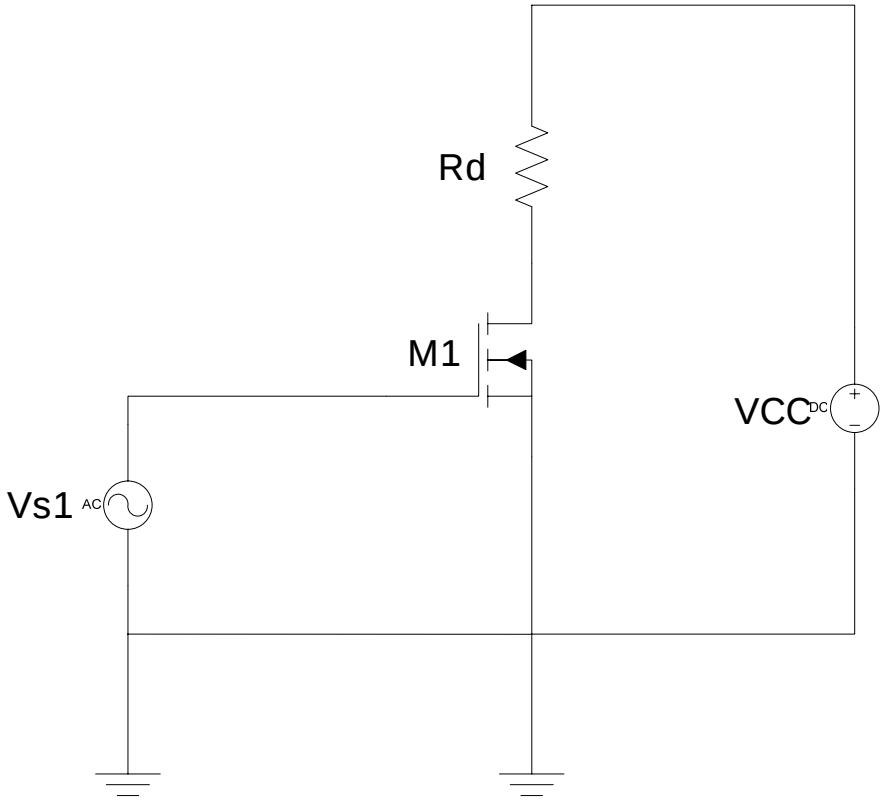
Spice Example 1 (1)

- **Circuit Schematic**



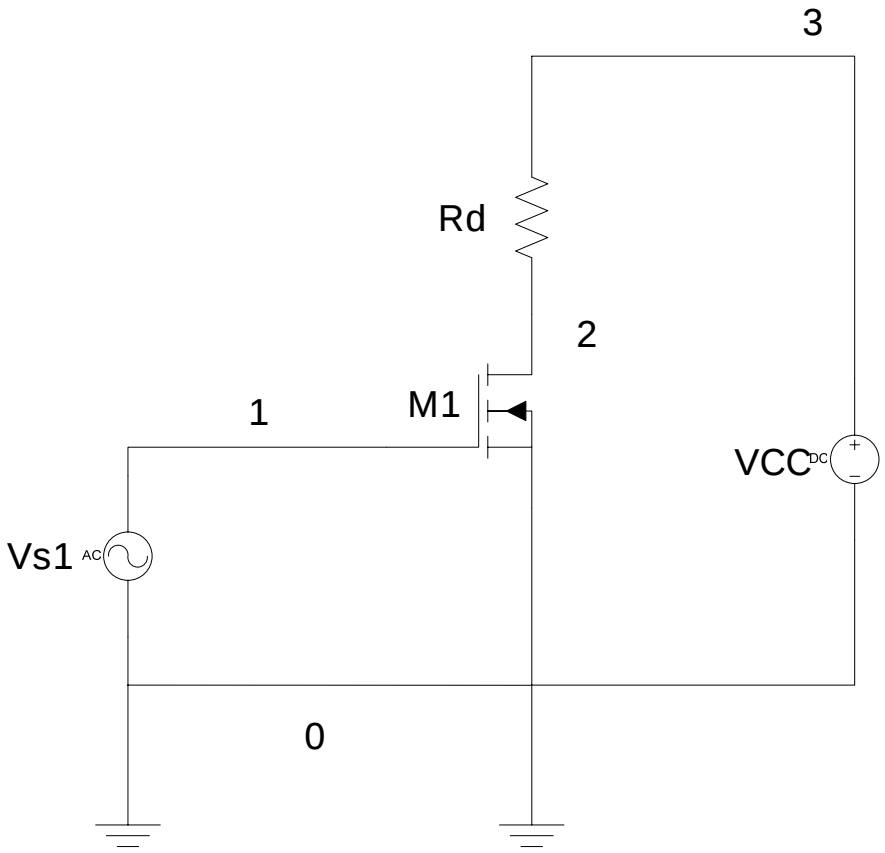
Spice Example 1 (2)

- **Identify Circuit Elements**



Spice Example 1 (3)

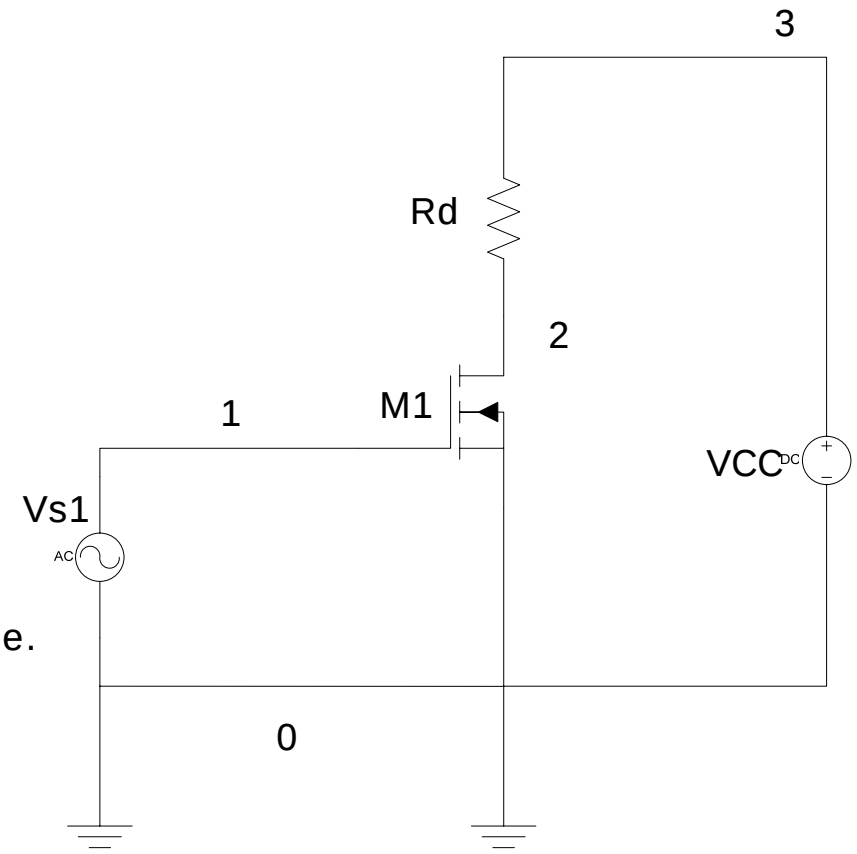
- **Identify Node Names**



Spice Example 1 (4)

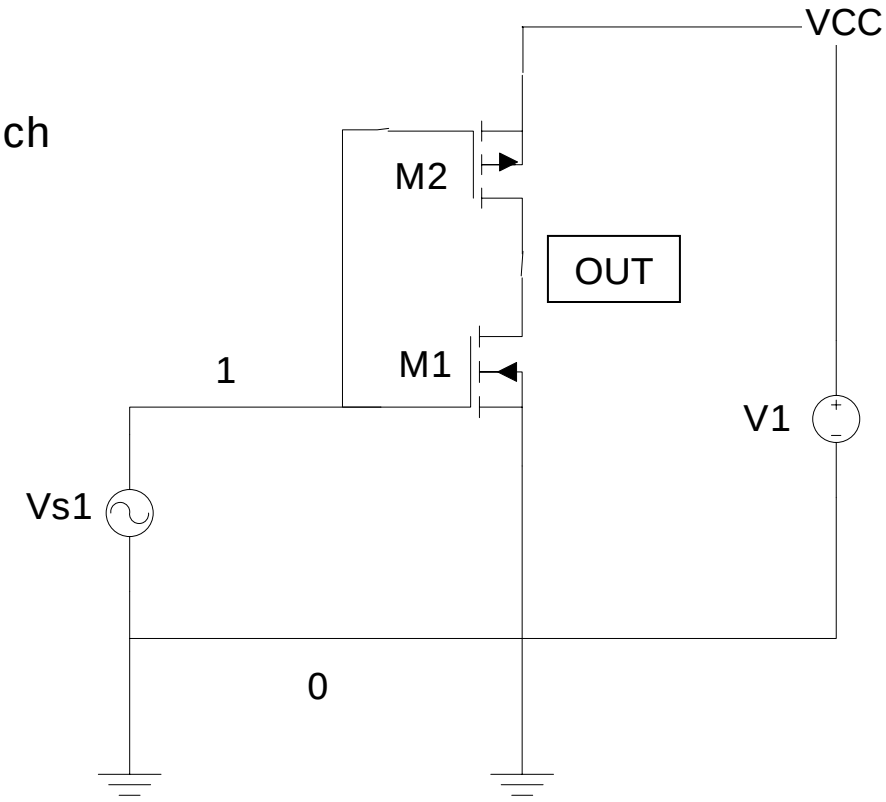
Writing the Netlist

```
*Sources
VCC 3 0 10V
Vs1 1 0 SIN (5V 2.5V 50)

*Elements
M1 2 1 0 0 nmos_330 L=20u W=100u
Rd 3 2 10k

*Model statements
.MODEL nmos_330 nmos (kp=20u
+Vto=+1V lambda=0.1)
*In the case of continuation in the
*new line use '+' at the first of new line.

*Analysis requests
.TRAN 1m 5 0 1m
.PROBE
.END
```



Spice Example 2 (1)

- Identify circuit elements.
- Identify node names.
  - A Node name can be alphabetically named, such as VCC and VSS.



Spice Example 2 (2)

Netlist

```
*Sources
V1 VCC 0 10V
Vs1 1 0 SIN (5V 2.5V 50)
*Elements
M1 OUT 1 0 0 nmos_330 L=20u W=100u
M2 OUT 1 VCC VCC pmos_330 L=20u
+W=400u

*Model statements
.MODEL nmos_330 nmos (kp=20u
+Vto=+1V lambda=0.1)
.MODEL pmos_330 pmos (kp=20u
+Vto=-1V lambda=0.1)

*Analysis requests
.TRAN 1m 5 0 1m
.PROBE
.END
```