Course Evaluation

- On line course evaluation
- Accessible through WebCT account

ECSE-330: Introduction to Electronics
Winter Session, 2008

What You Already Know (ECSE-210)

- Circuit models – resistors, capacitors, inductors
- KVL and KCL
- Branch relationships
- Resistive circuit analysis
- Network theorems including one and two port networks
- Steady state, transient and frequency analysis

What Was Covered

Chapter 1) ***Introduction to Analog and Digital Electronics***

Sections 1.4-1.7

Chapter 3) ***The PN Junction and Diodes***

Sections 3.1-3.7

Chapter 4) ***Field-Effect Transistors***

Sections 4.1-4.10, (also 10.3, 6.3)

Chapter 5) ***Bipolar Junction Transistors***

Sections 5.1-5.10, (also 6.3)

Chapter 2 was NOT covered

Upon Completion of the Course

- Design and analysis of circuits:
  - *Rectify signals* – diodes
  - *Amplify signals* – analog functions
  - *Digital circuits* – digital signal processing
- Design principles behind the realization of modern *Integrated Circuits (ICs)*
- An understanding of physical principles behind the operation of transistors and diodes
- Everything you need to know for ECSE-334, Electronic Circuits II.

Outline of Chapter 1

Analog Amplifiers

- Linear amplifiers and transfer characteristics
- Classification of ideal amplifier topologies and desirable properties
- Input/Output resistance

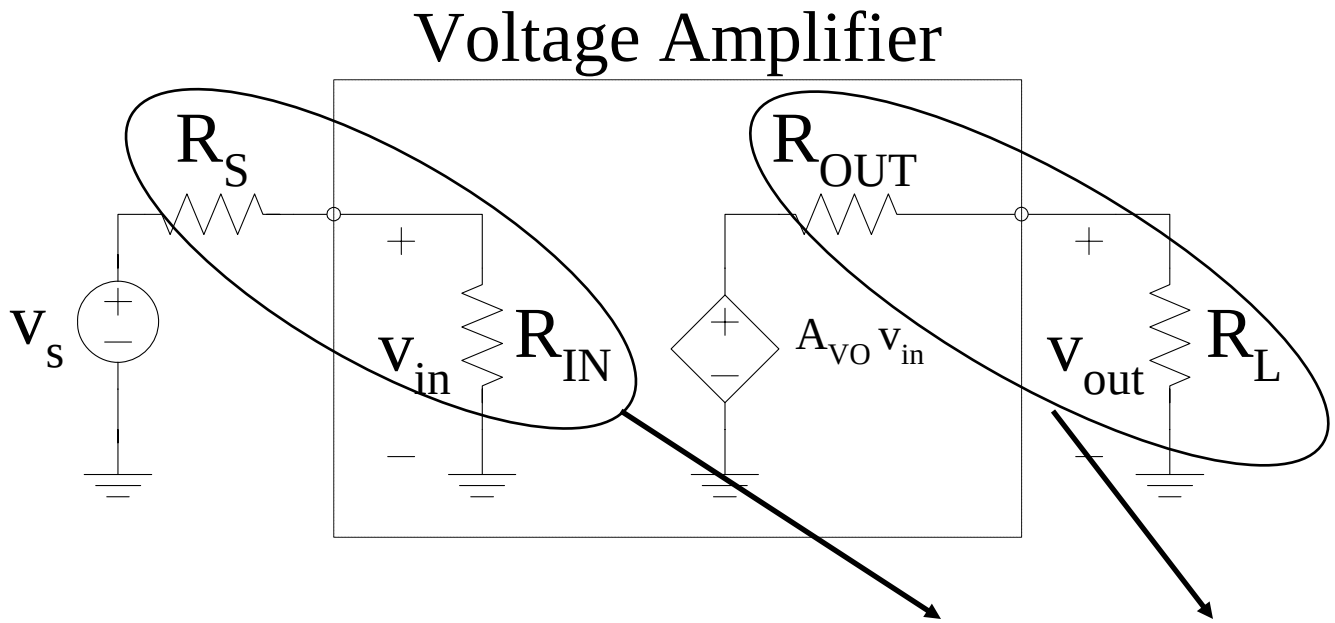
Digital Logic Inverters

- Voltage transfer characteristic
- Noise margins

Frequency Response

- STC circuits
- Transfer function
- Bode plots

Attach Source and Output Loads



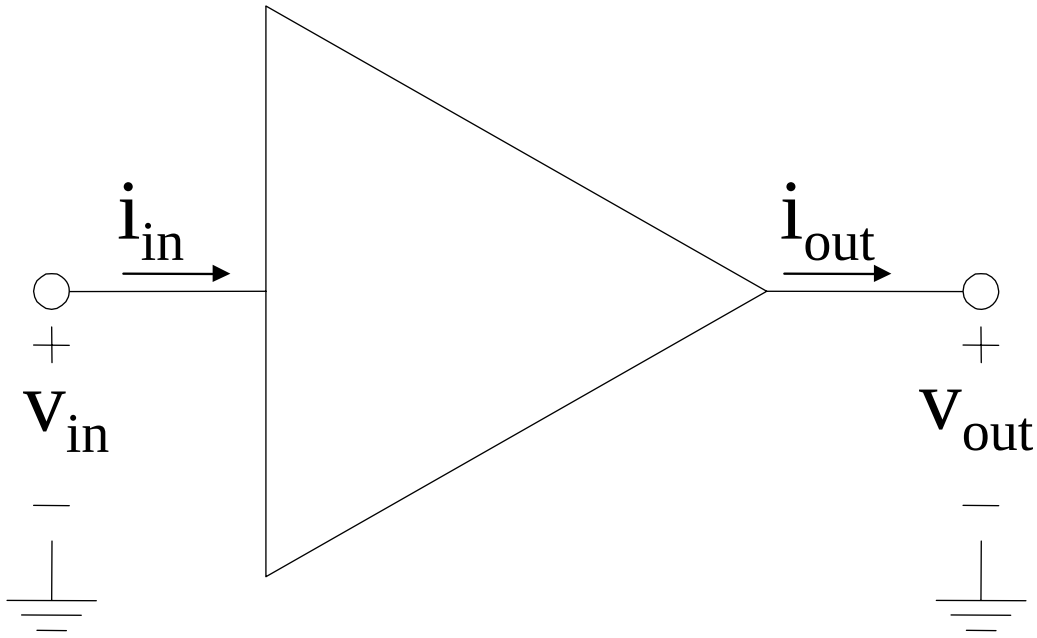
Compute Voltage Gain: $A_V = \frac{v_{out}}{v_s} = \frac{R_{IN}}{R_{IN}+R_S} \cdot \frac{R_L}{R_L+R_{OUT}} \cdot A_{VO}$

1) $A_V < A_{VO}$ due to two voltage divisions: source and load
2) A_V maximized with large R_{IN}, small R_{OUT}

Finding R_{IN}

R_{IN} is the resistance "seen" between the input node and ground

With input signal applied, v_{in} and i_{in} signals are established

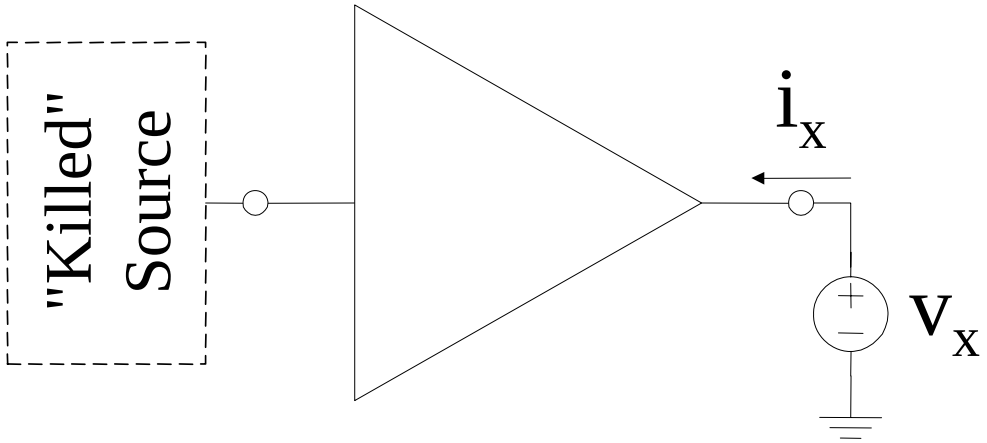


$$R_{IN} = \frac{v_{in}}{i_{in}}$$

Important:
R_{IN} can usually be obtained by inspection

Finding R_{OUT}

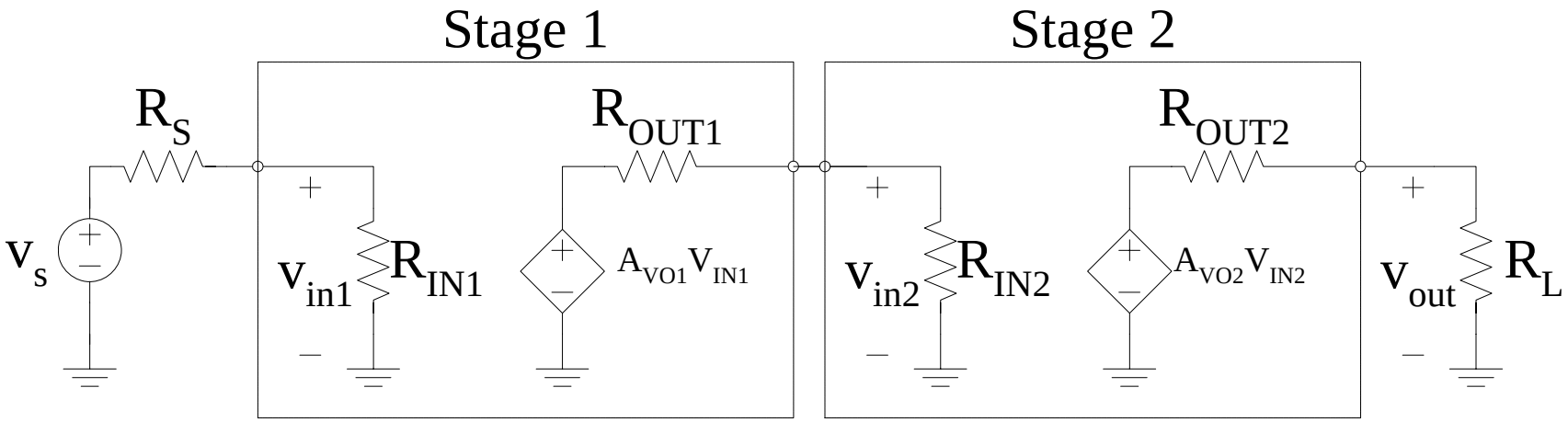
- Alternatively, one can determine R_{OUT} as follows:
  - "Kill" the input signal (set v_{in} or i_{in} to zero)
  - Apply a test voltage signal v_x to the output node
  - Determine the current i_x it supplies to the circuit



$$R_{OUT} = \frac{v_x}{i_x}$$

Cascaded Amplifier Stages

- e.g. cascaded voltage amplifiers:



- By inspection, working from output to input:

$$A_V = \frac{v_{out}}{v_s} = \frac{R_L}{R_L + R_{OUT2}} \cdot A_{VO2} \cdot \frac{R_{IN2}}{R_{IN2} + R_{OUT1}} \cdot A_{VO1} \cdot \frac{R_{IN1}}{R_{IN1} + R_S}$$

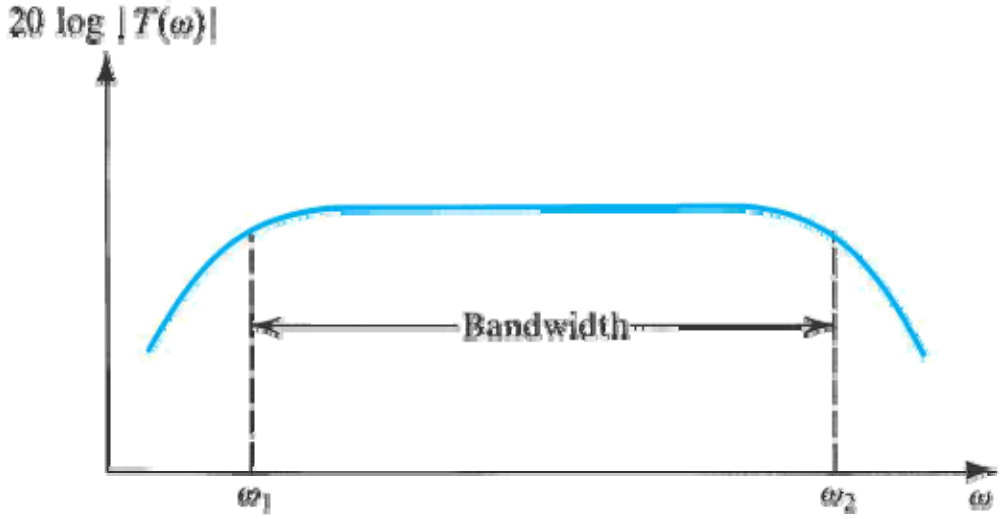
- Equally simple for other amplifier cascades

Measuring Frequency Response

- The **frequency response** of an amplifier is completely known by the **magnitude (or amplitude) response** and **phase response**

$$|T(\omega)| = \frac{V_o}{V_i} \qquad \angle T(\omega) = \phi$$

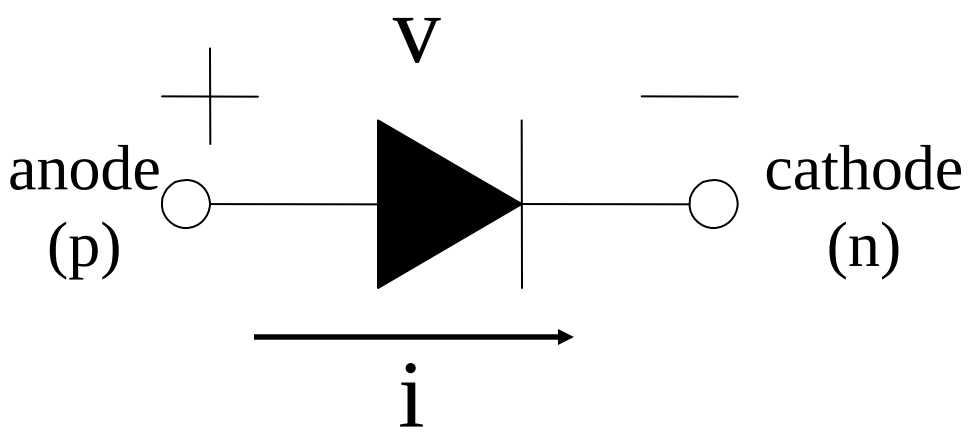
- Often the magnitude plot is given in decibels and **20log|*T(ω)*|** is plotted versus frequency



Outline of Chapter 3 - Diodes

- Exponential model
- Constant voltage drop model
- Applications
- Small-signal model
- PN junctions

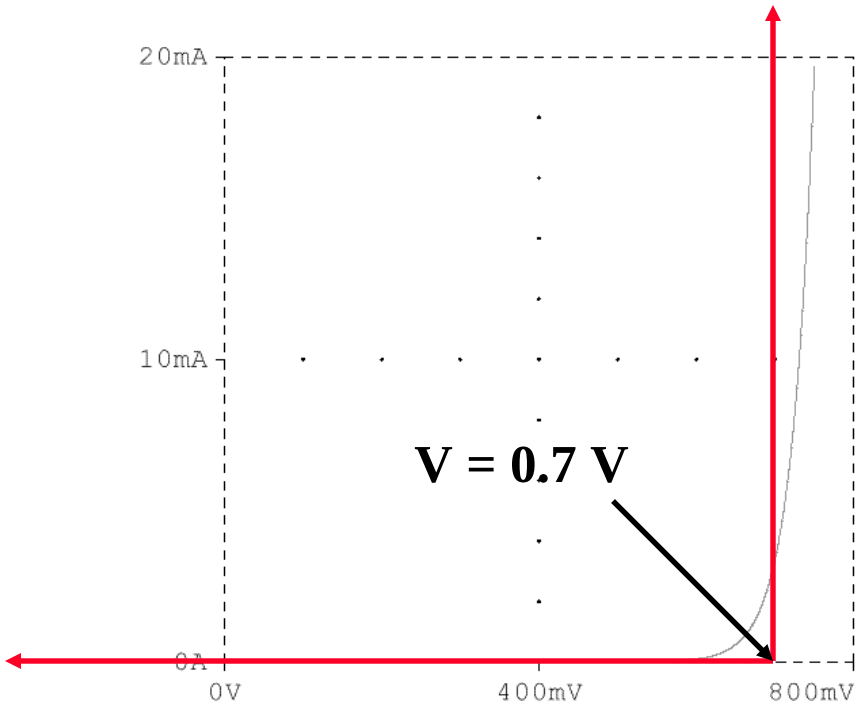
Diode Symbol and Terminal Characteristics



Exponential model: $i = I_S\left(e^{\frac{v}{nV_T}} - 1\right)$

The Constant Voltage Drop Model (CVDM)

- Exponential model gives accurate results; requires hand computation or a simulator
- The constant voltage drop model (CVDM) used to perform quick analysis of a diode circuit by hand
- CVDM approximates diode I-V curve piecewise-linearly



Small-Signal Analysis Technique Summary

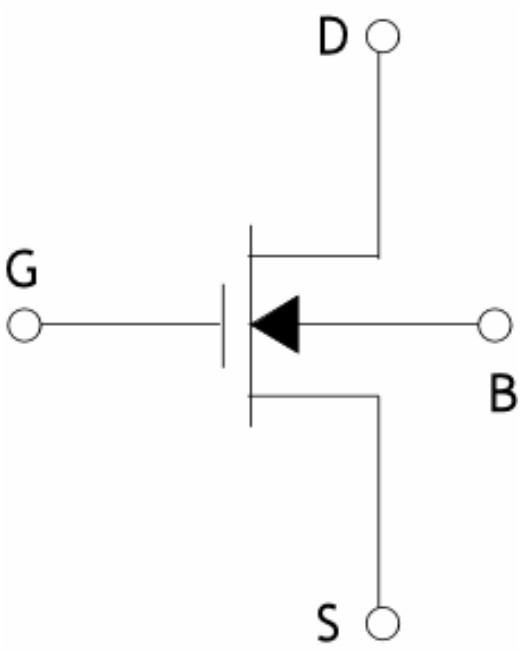
- Tool for analyzing the behavior of circuits that employ active devices and small signals
- Through linearization of exponential model, can separate DC & AC analysis; linear superposition
- Analysis procedure
  - Turn off AC sources, solve for DC operating point
  - Based on DC operating point parameters, solve for small signal-signal equivalent circuit model parameters
  - Construct small-signal equivalent circuit; short circuit voltage sources and open circuit current sources
  - Solve for AC parameters

Outline of Chapter 4

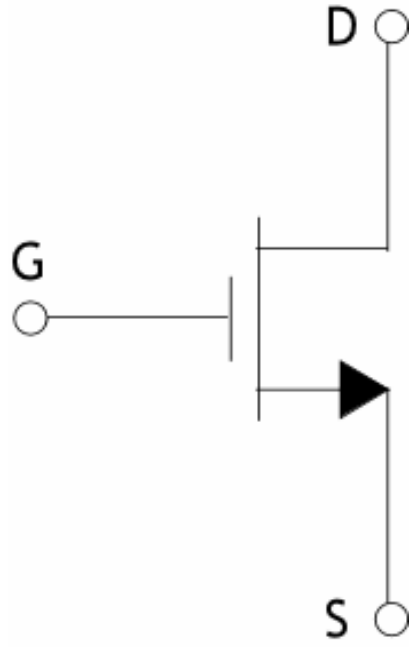
- Introduction to MOS Field Effect Transistor (MOSFET)
- NMOS FET
- PMOS FET
- DC Analysis of MOSFET Circuits
- MOSFET Amplifier
- MOSFET Small Signal Model
- MOSFET Integrated Circuits
- CSA, CGA, CDA
- CMOS Inverter & MOS Digital Logic
- High frequency model and Frequency response of CSA

nMOS Circuit Symbol

- A MOSFET is a ***four-terminal*** device
- Body terminal ***always*** biased at ***most negative*** potential

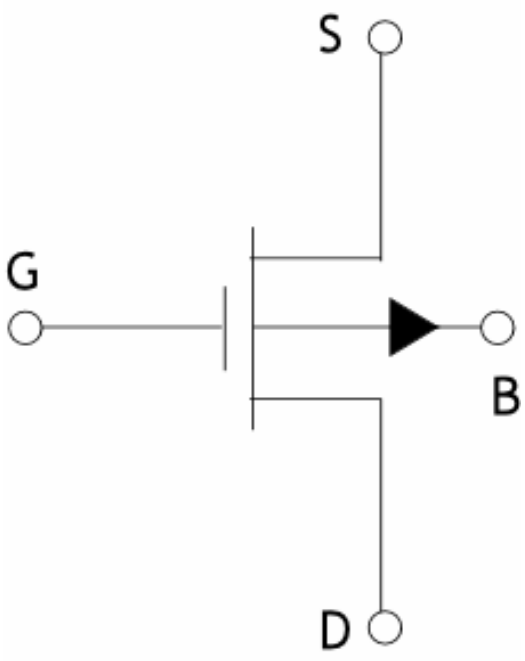


- Simplified symbol with implicit Body terminal connection
- Arrow indicates direction of current

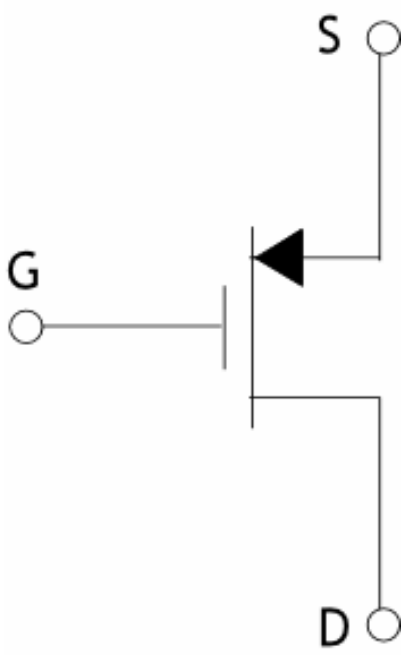


pMOS Circuit Symbol

- A MOSFET is a ***four terminal*** device
- Body terminal ***always*** biased at ***most positive*** potential



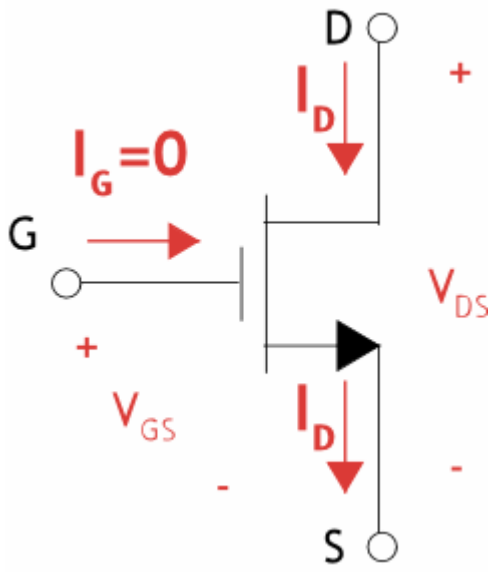
- Simplified symbol with implicit Body terminal connection
- Arrow indicates direction of current flow



Summary of Enhancement nMOS FET I-V Characteristics

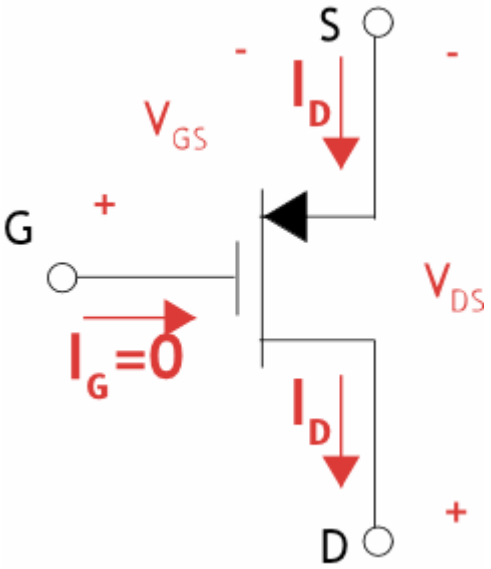
Cutoff:	$V_{GS} < V_t$	$I_D = 0$
Triode:	$V_{GS} > V_t$ $V_{DS} < V_{GS} - V_t$	$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$
Saturation:	$V_{GS} > V_t$ $V_{DS} > V_{GS} - V_t$	$I_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$

Body effect: $V_t = V_{t0} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right)$



Summary of pMOS FET I-V Characteristics

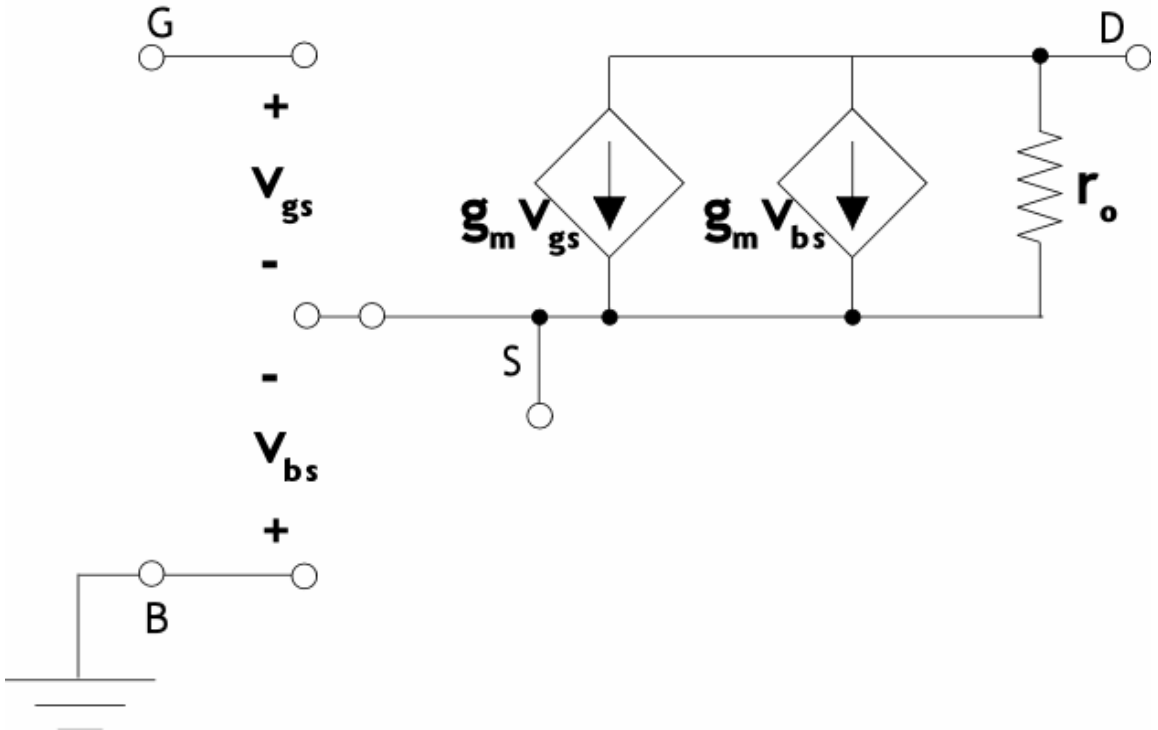
Cutoff:	$V_{GS} > V_t$	$I_D = 0$
Triode:	$V_{GS} < V_t$ $V_{DS} > V_{GS} - V_t$	$I_D = k'_p \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$
Saturation:	$V_{GS} < V_t$ $V_{DS} < V_{GS} - V_t$	$I_D = \frac{1}{2}k'_p \frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$



Body effect: $|V_t| = |V_{t0}| + \gamma\left(\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f}\right)$

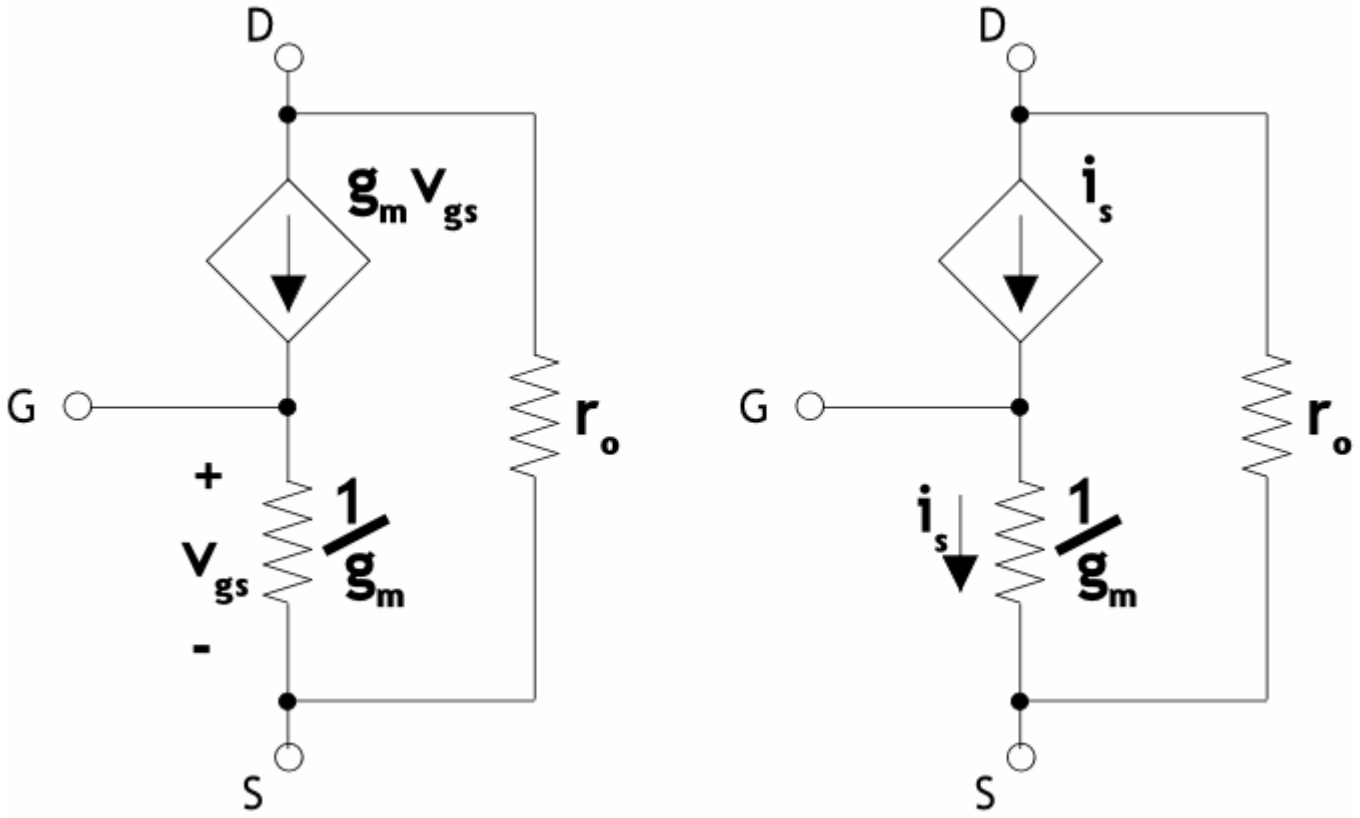
Note: V_{GS}, V_{DS}, V_{SB}, V_t, λ, are all NEGATIVE

Hybrid-π Small Signal Model



- AC Body effect: another VCCS (dependent on g_{mb}) in parallel with the one dependent on g_m
- T model generally not used when modeling Body effect, regardless of circuit topology

The MOSFET T Small Signal Model

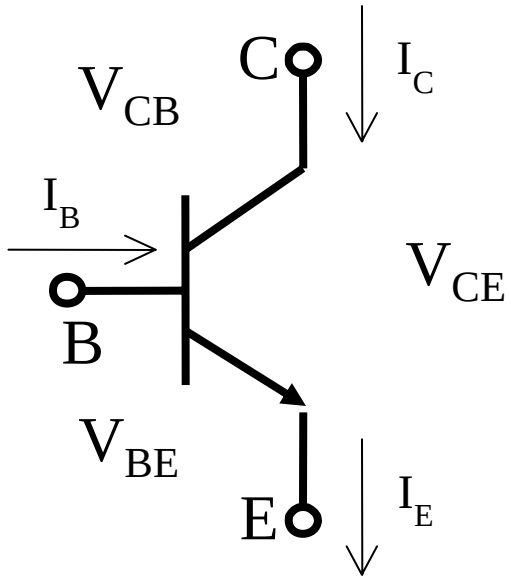


Outline of Chapter 5

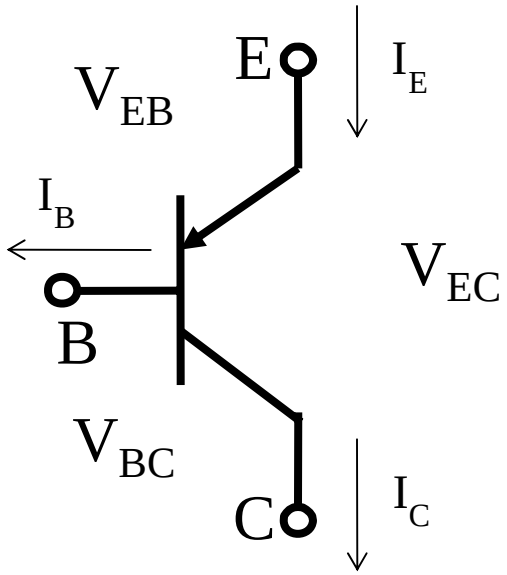
- Introduction to The Bipolar Junction Transistor
- Active Mode Operation of the npn and pnp BJTs
- DC Analysis of BJT Circuits
- BJT as an Amplifier
- BJT Small Signal Models
- CEA, CEA with R_E, CBA, & CCA
- Integrated Circuit Amplifiers
- High-frequency model and frequency response

Bipolar Junction Transistor (BJT)

- 3 terminal device in which the voltage across 2 terminals controls the current flowing in/out of a 3rd terminal:



npn BJT



pnp BJT

Summary of npn Active Mode Characteristics

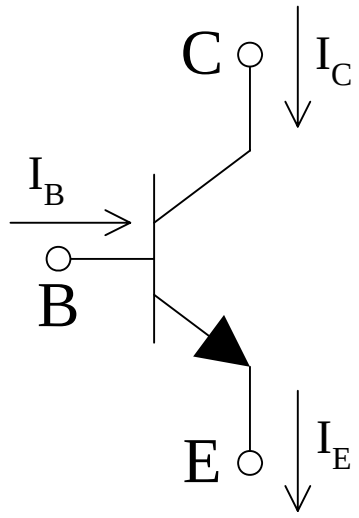
$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)\left(1+\frac{V_{CE}}{V_A}\right)$$

$$I_B = \frac{I_C}{\beta} \qquad r_o = \frac{V_A}{I_C}$$

$$I_C = \alpha I_E; \qquad \alpha = \frac{\beta}{\beta+1} \approx 1$$

$$I_E = (\beta+1) I_B$$

$$I_E = I_C + I_B$$



$$V_C \geq V_B > V_E; \quad V_{BE} \approx 0.7V$$

Summary of pnp Active Mode Characteristics

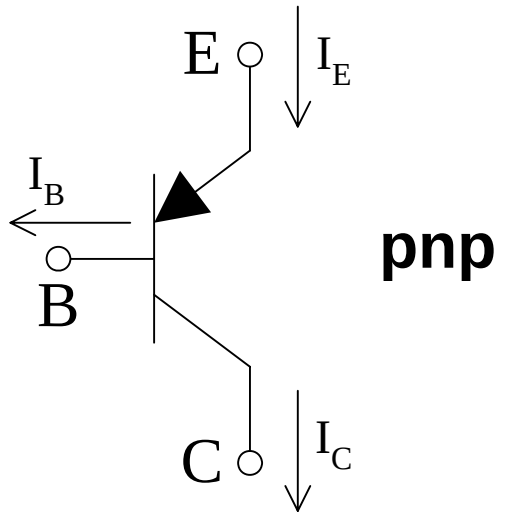
$$I_C = I_S \exp\left(\frac{V_{EB}}{V_T}\right)\left(1+\frac{V_{EC}}{V_A}\right)$$

$$I_B = \frac{I_C}{\beta} \qquad r_o = \frac{V_A}{I_C}$$

$$I_C = \alpha I_E; \qquad \alpha = \frac{\beta}{\beta+1} \approx 1$$

$$I_E = (\beta+1) I_B$$

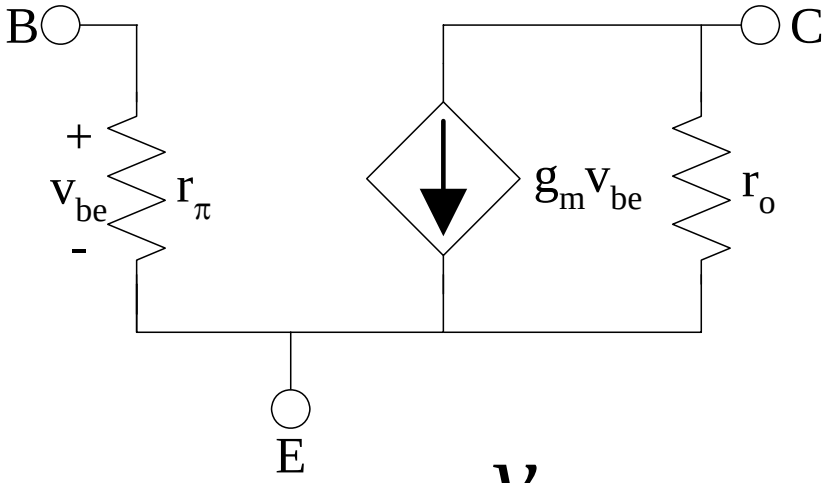
$$I_E = I_C + I_B$$



$$V_E \geq V_B > V_C; \quad V_{EB} \approx 0.7V$$

Hybrid-π Small Signal Models

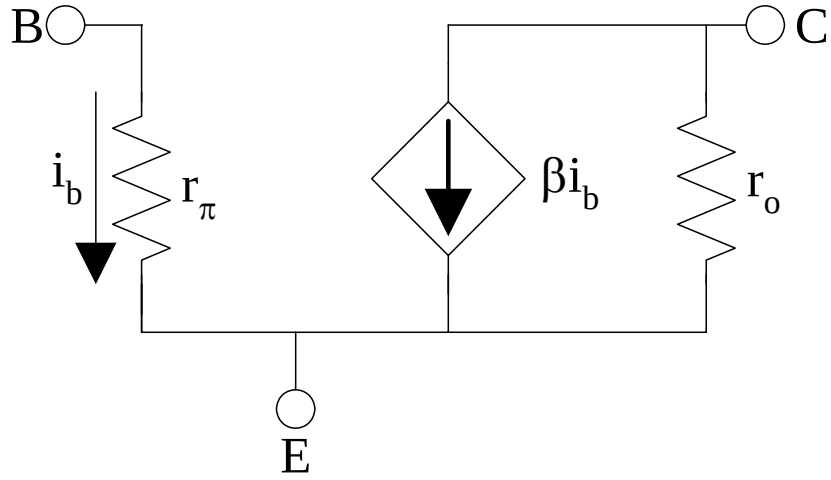
VCCS based model



$$i_b = \frac{v_{be}}{r_\pi}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{V_T}{I_B}$$

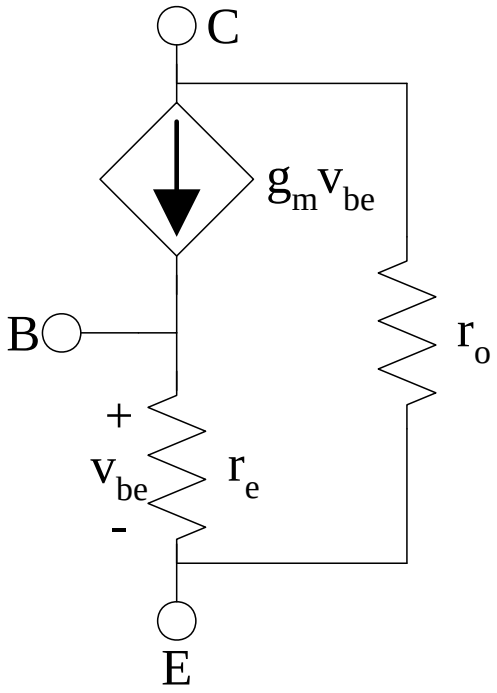
CCCS based model



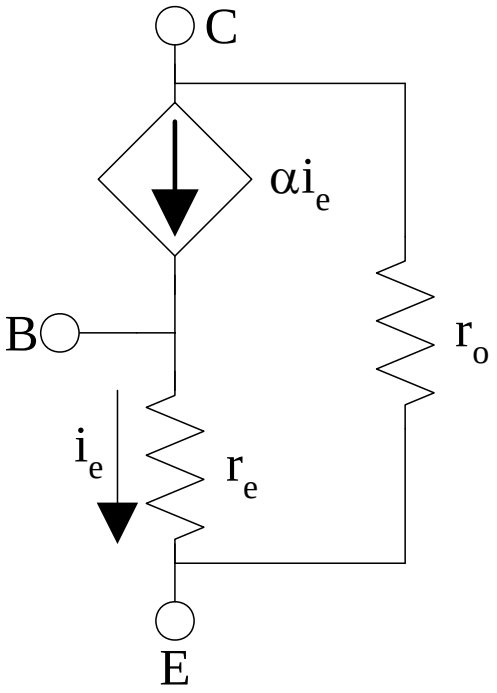
$$g_m v_{be} = (g_m r_\pi) i_b = \beta i_b$$

T-Models

VCCS based model



CCCS based model

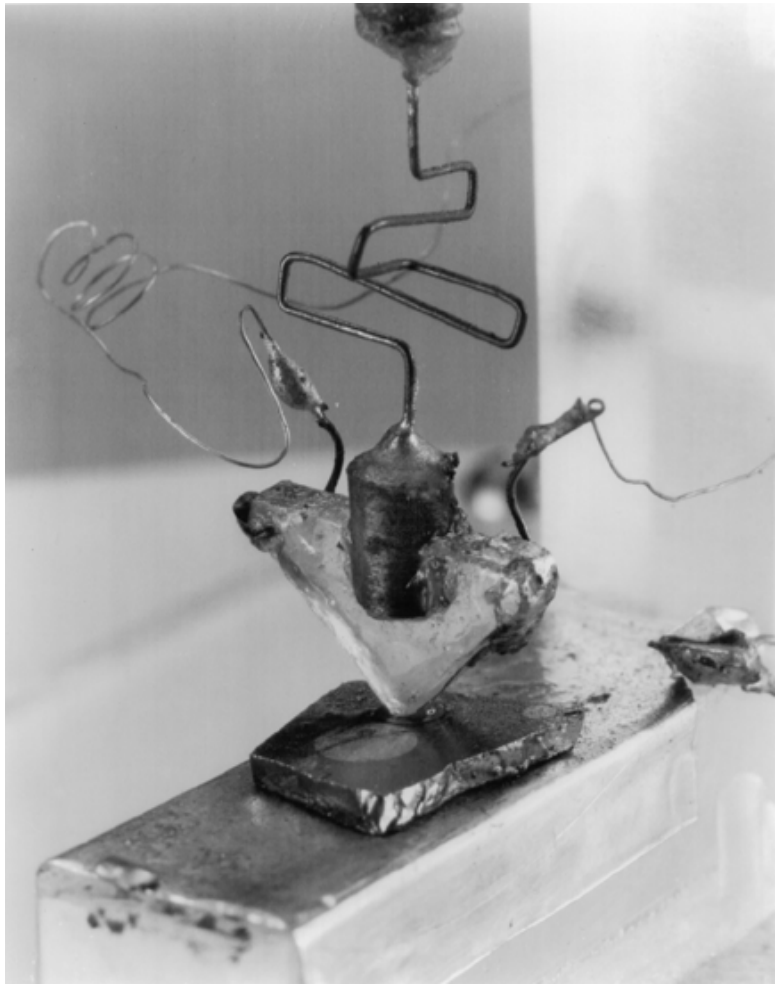


$$i_e = \frac{v_{be}}{r_e} \qquad r_e = \frac{\alpha}{g_m} = \frac{V_T}{I_E}$$

$$g_m v_{be} = (g_m r_e) i_e = \alpha i_e$$

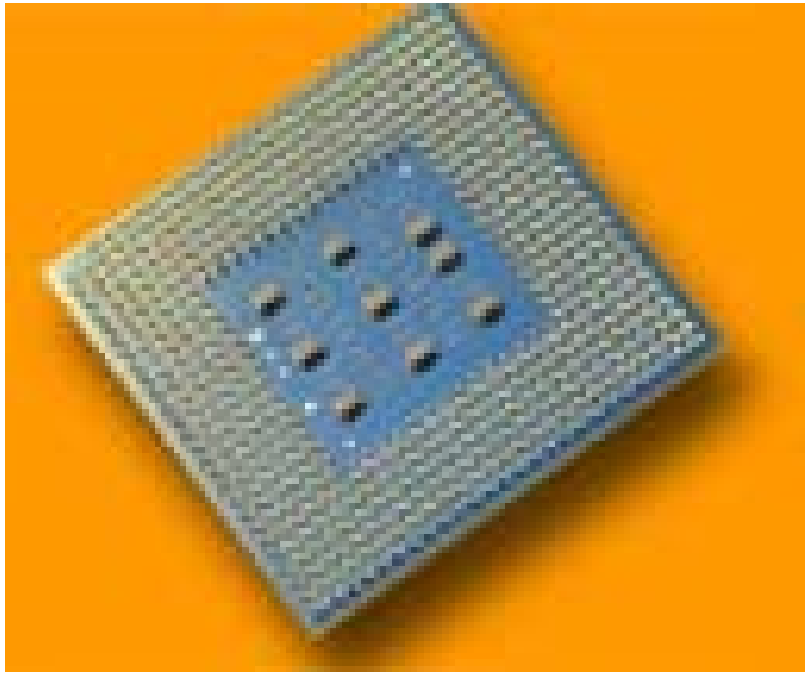
Beginning of the Transistor Era

- 1st transistor – invented in 1947 at Bell Laboratories.
- Invented by Brattain and Bardeen.
- PNP point-contact germanium transistor.
- Operated as a speech amplifier with a power gain of 18.



And now?

- The Pentium IV with 55 million transistors
- These transistors are located in an area of ~12 mm x 12 mm
- 0.13µm technology, 0.09µm technology is also available



And now?

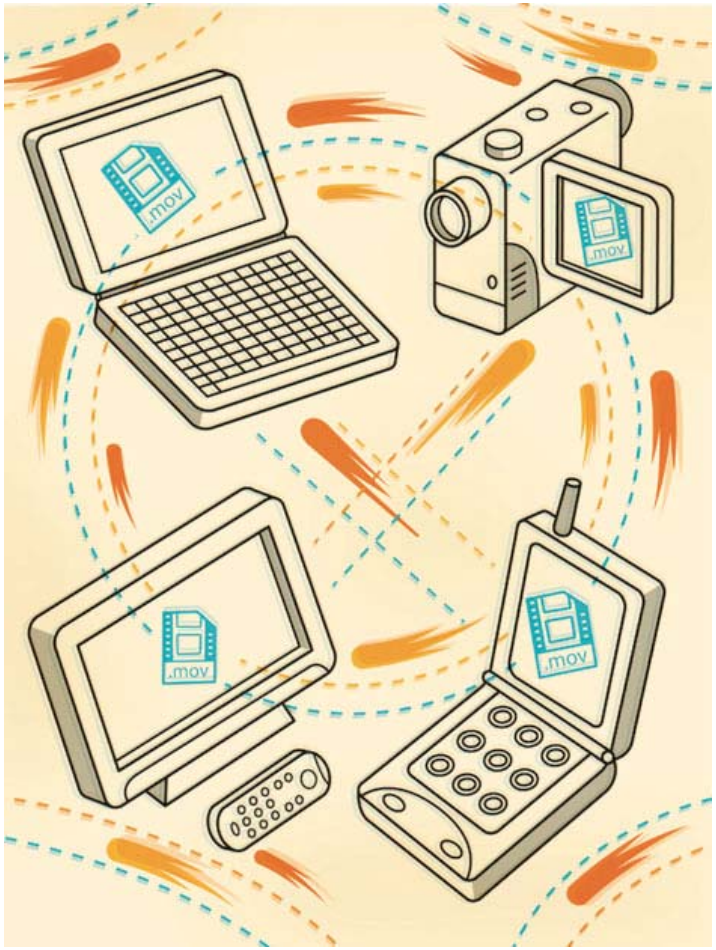
- Feb. 2005, *IEEE International Solid-State Conference (ISSCC)*

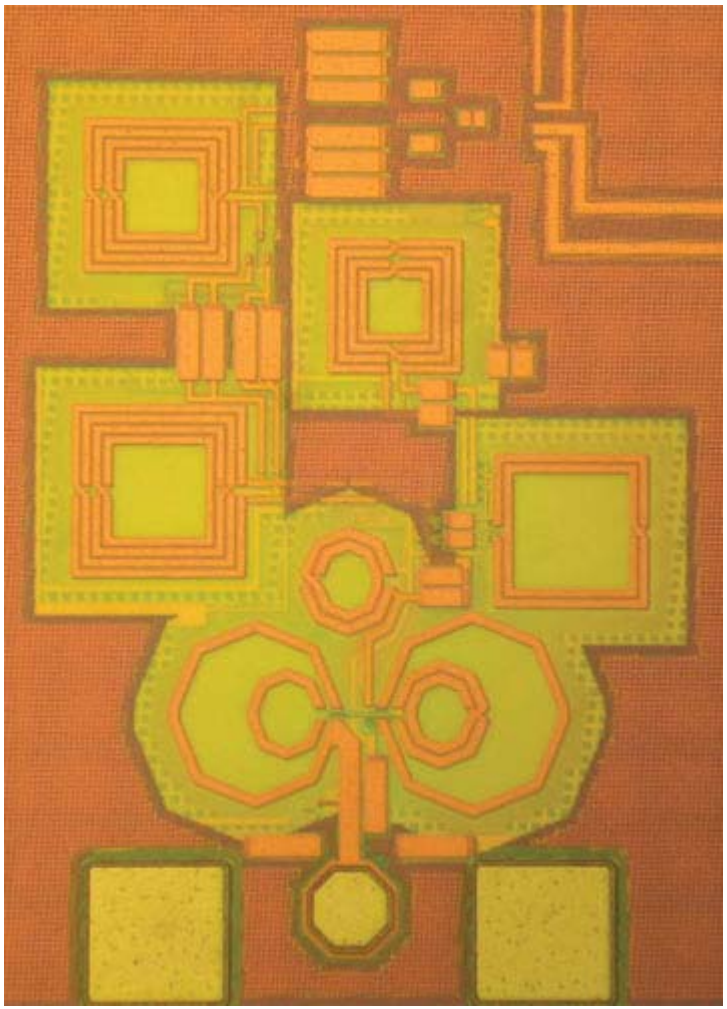
➢ CELL Processor (designed and developed by SONY, Toshiba, IBM):
  – The first consumer exposure was in Sony's PlayStation 3 game console
  – 4 GHz, 1.1V Vdd, BGA package (42.5 mm by 42.5 mm), 90 nm process
  – One sample operate at 5.6 GHz with 1.4V Vdd

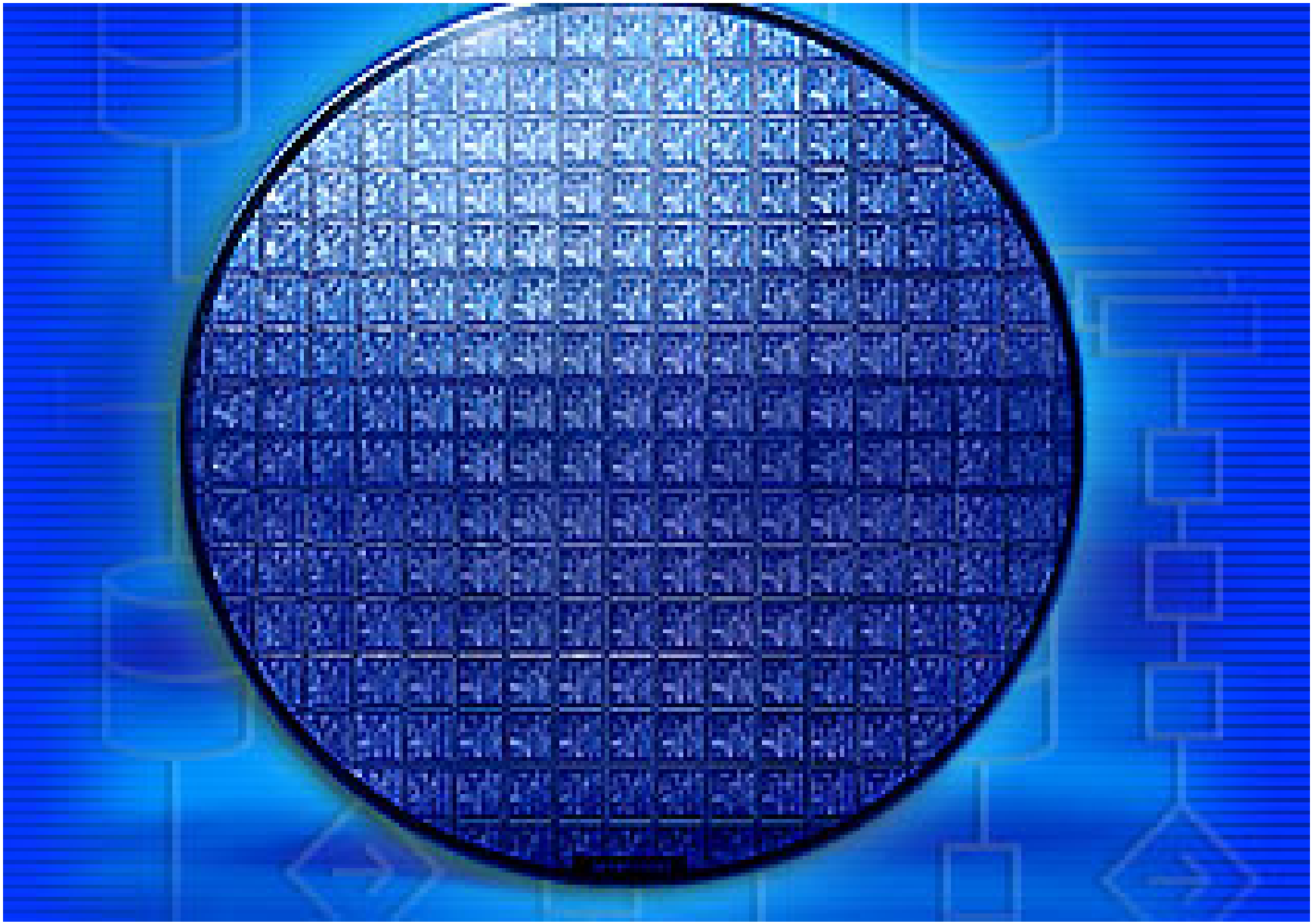
➢ CMOS used for short-range wireless communications at 60 GHz, 0.13μm technology
  – Wireless-LAN ICs delivered as single-chip solutions, built in CMOS at foundries in Taiwan.
  – Texas Instruments Inc. shakes up the cost-sensitive handset market with baseband-plus-RF parts made in 90-nanometer CMOS.

Near Future

- We want to develop Personal Area Networks using CMOS wireless electronics







Final Exam Topics

- Amplifiers
  - General amplifier analysis and frequency response
- Diodes:
  - DC analysis including exponential and CVD
  - Small signal analysis including diode small signal resistance
  - Applications and circuits
- FETs:
  - NMOS, PMOS
  - DC analysis
  - Cut-off/triode/saturation behavior
  - Small signal modeling including CSA, CGA, CDA
  - Multistage amplifiers
  - Body effect and Channel Length Modulation (DC and small signal)
  - Current mirrors – DC and small signal
  - High frequency model and frequency response of CSA

Final Exam Topics

- BJTs:
  - NPN, PNP
  - DC analysis
  - Cut-off/saturation/active behavior
  - Small signal modeling including CEA, CEA with RE, CBA, CCA
  - Early effect
  - Multistage amplifiers
  - Current mirrors – DC and small signal
  - High frequency model and frequency response of CEA

  All topics including physics, derivations, problem solving and numerical calculation

ECSE-330: Electronic Circuits I
Winter Session, 2008

Good Luck,

and

Have a great

Summer!