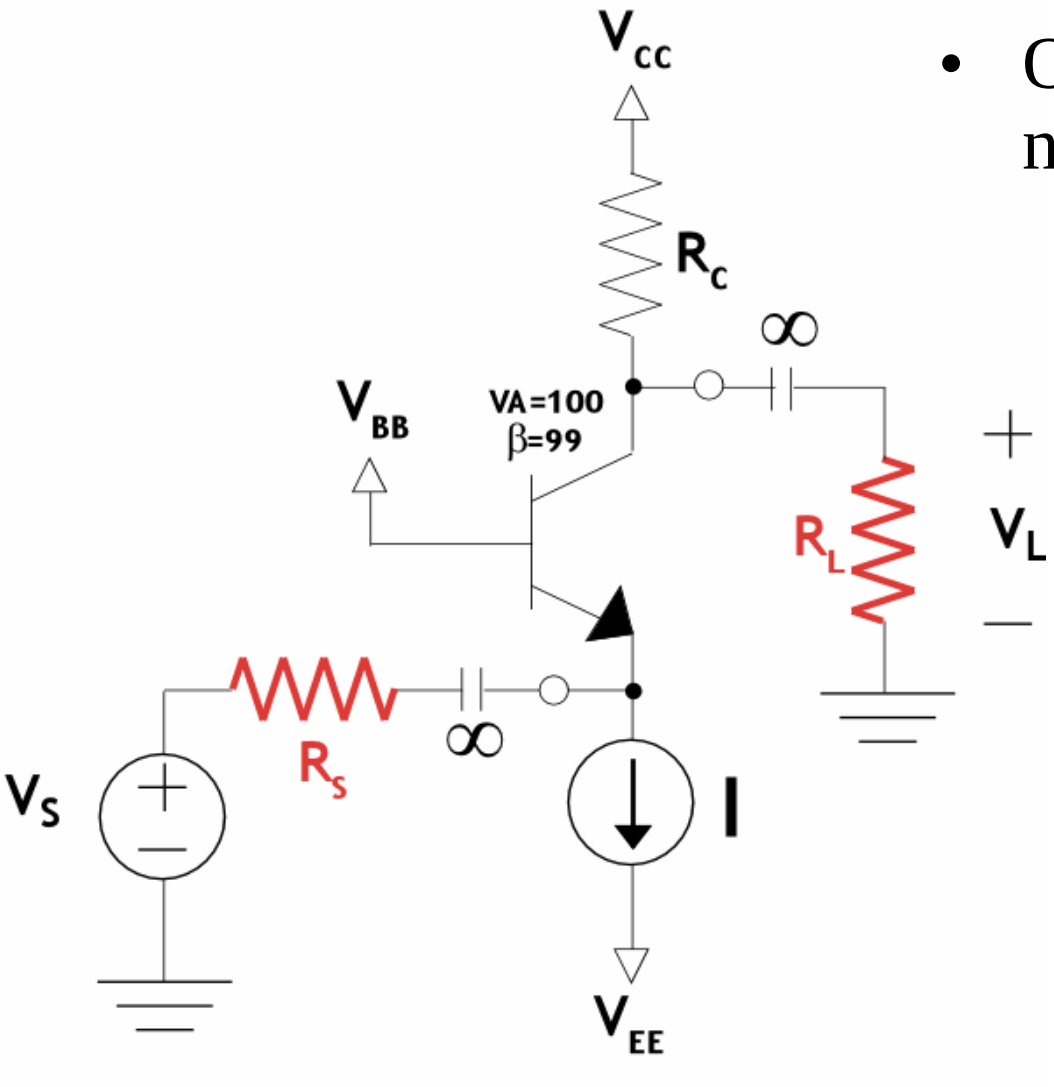
Outline of Chapter 5

- 1- Introduction to The Bipolar Junction Transistor
- 2- Active Mode Operation of BJT
- 3- DC Analysis of Active Mode BJT Circuits
- 4- BJT as an Amplifier
- 5- BJT Small Signal Models
- 6- CEA, CEA with R_E, CBA, & CCA
- 7- Integrated Circuit Amplifiers

CBA with r_o (Resistance Coupling C-E)



- Original results neglecting R_S, R_L, & r_o:

Open circuit voltage gain

$$A_{VO} = \frac{v_{out}}{v_{in}} = g_m R_C$$

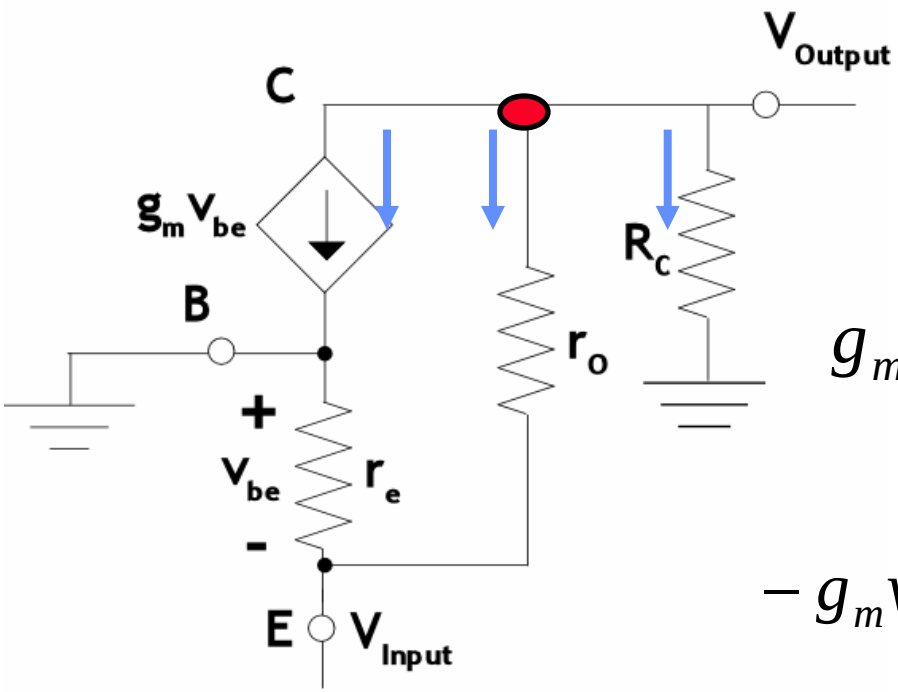
Short circuit current gain

$$A_{IS} = \frac{i_{out}}{i_{in}} = \alpha$$

$$R_{IN} = r_e$$

$$R_{OUT} = R_C$$

CBA with r_o-Voltage Gain



$$v_{be} = -v_{Input}$$

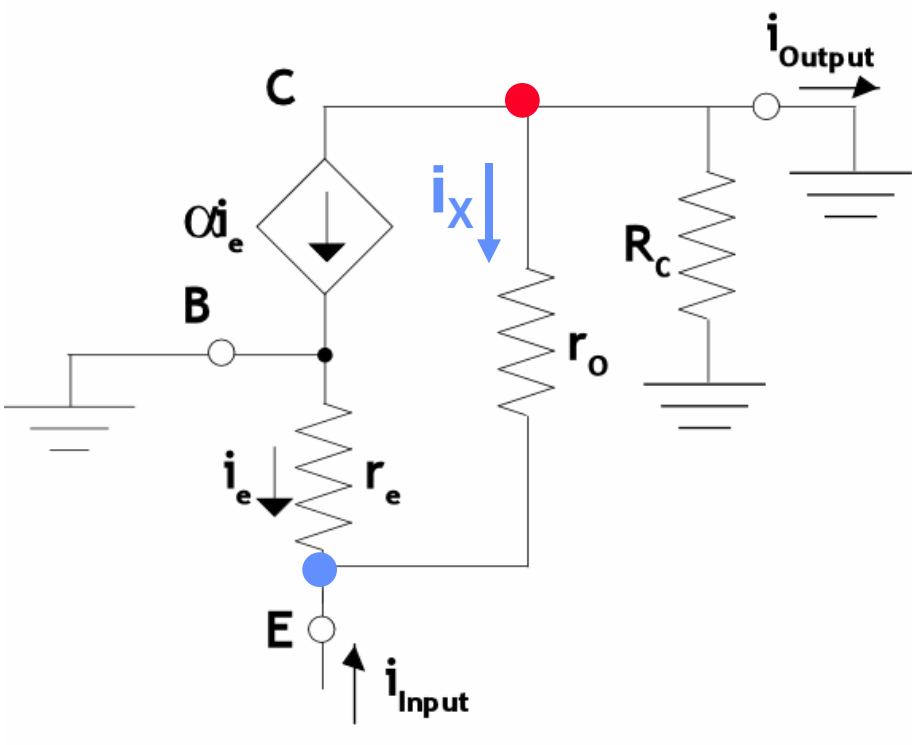
$$g_m v_{be} + \frac{(v_{Output} - v_{Input})}{r_O} + \frac{v_{Output}}{R_C} = 0$$

$$-g_m v_{Input} + \frac{(v_{Output} - v_{Input})}{r_O} + \frac{v_{Output}}{R_C} = 0$$

$$\boxed{A_{VO} = \left(g_m + \frac{1}{r_o}\right)\left(r_o \| R_C\right)}$$

Large r_o has little effect on gain

CBA with r_o Short-Circuit Current Gain



$$\alpha i_e + i_x + i_{Output} = 0$$

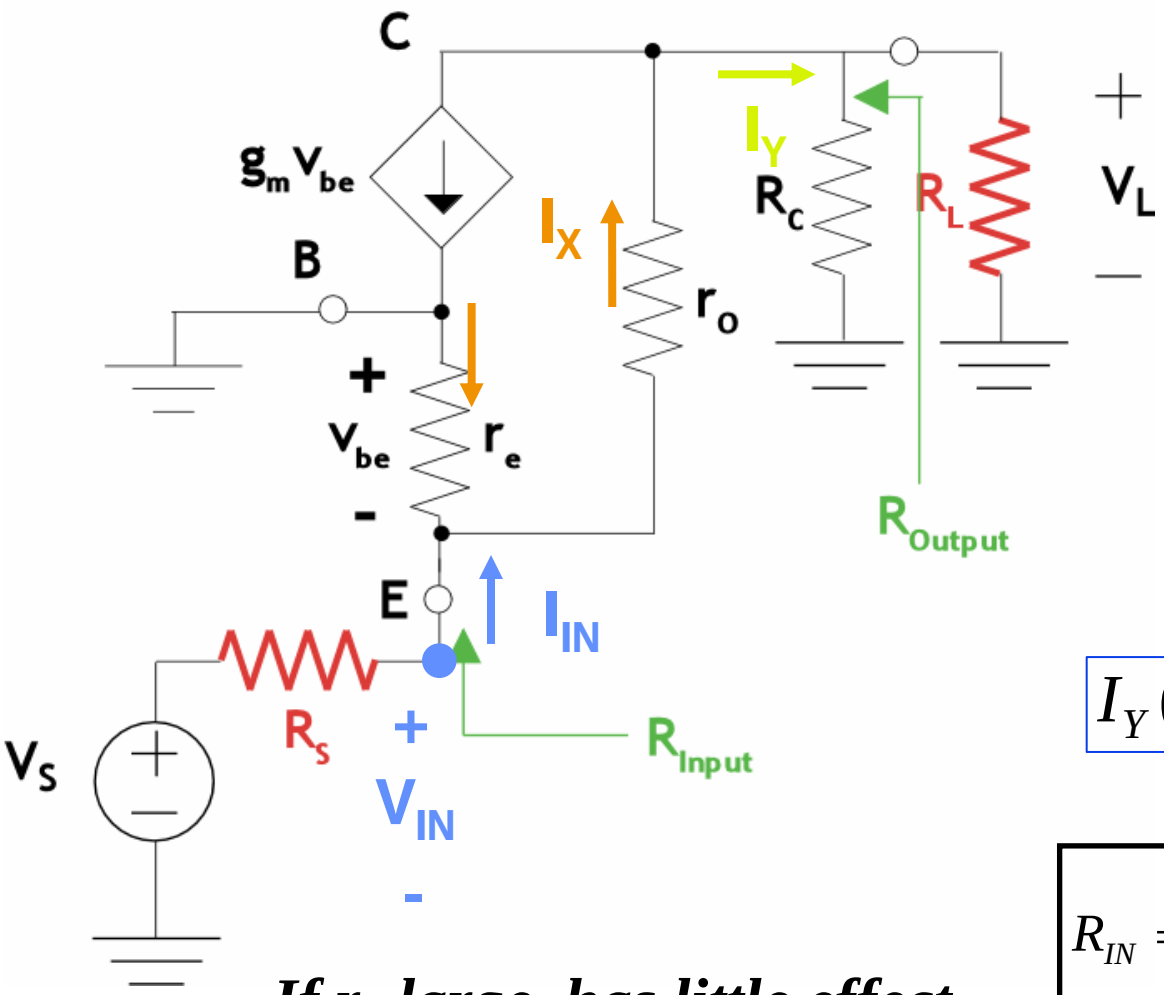
$$-i_{Input} - i_e - i_x = 0$$

$$i_e r_e = i_x r_O$$

$$A_{IS} = \frac{i_{out}}{i_{in}} = \frac{\alpha + r_e / r_o}{1 + r_e / r_o}$$

If r_o is large, it will have little effect on the overall gain

CBA with r_o-Input Resistance



$$R_{IN} = V_{IN} / I_{IN}$$

$$V_{IN} = -v_{be}$$

$$I_{IN} + \frac{v_{be}}{r_e} - I_X = 0$$

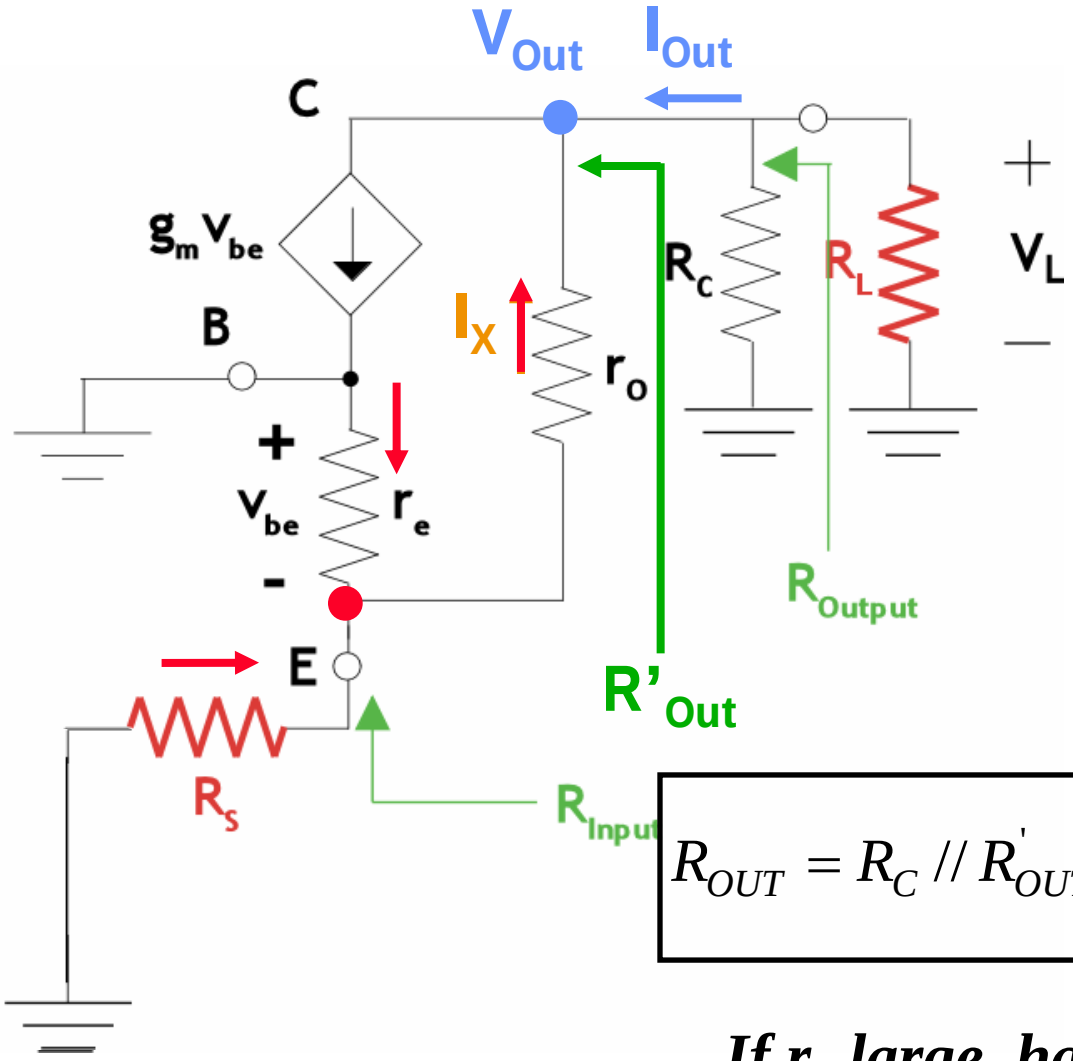
$$-g_m v_{be} + I_X - I_Y = 0$$

$$I_Y (R_C // R_L) + I_X r_0 + v_{be} = 0$$

$$R_{IN} = r_e \left\| \left[r_o \Big/ 1 - \left(g_m + \frac{1}{r_o} \right) \left(r_o \| R_C \| R_L \right) \right] \right.$$

If r_o large, has little effect

CBA with r_o-Output Resistance



$$R'_{Out} = V_{Out} / I_{Out}$$

$$-I_{Out} - g_m v_{be} + I_X = 0$$

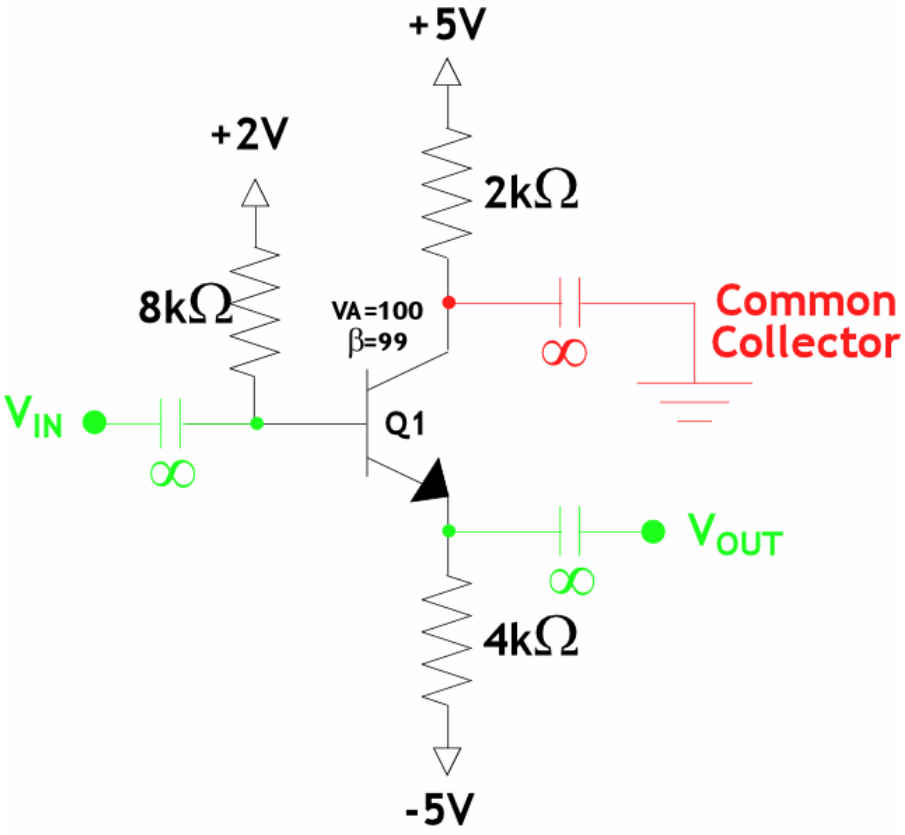
$$\frac{v_{be}}{r_e} + \frac{v_{be}}{R_S} - I_X = 0$$

$$I_X = \frac{(-V_{Out} + (-v_{be}))}{r_0}$$

$$R_{OUT} = R_C \,//\, R'_{OUT} = R_C \,//\, \frac{\left(r_o + r_e \| R_S\right)}{1 + g_m\left(r_e \| R_S\right)} \approx R_C \| \frac{r_o}{2}$$

If r_o large, has little effect

CCA Operation – Voltage Buffer



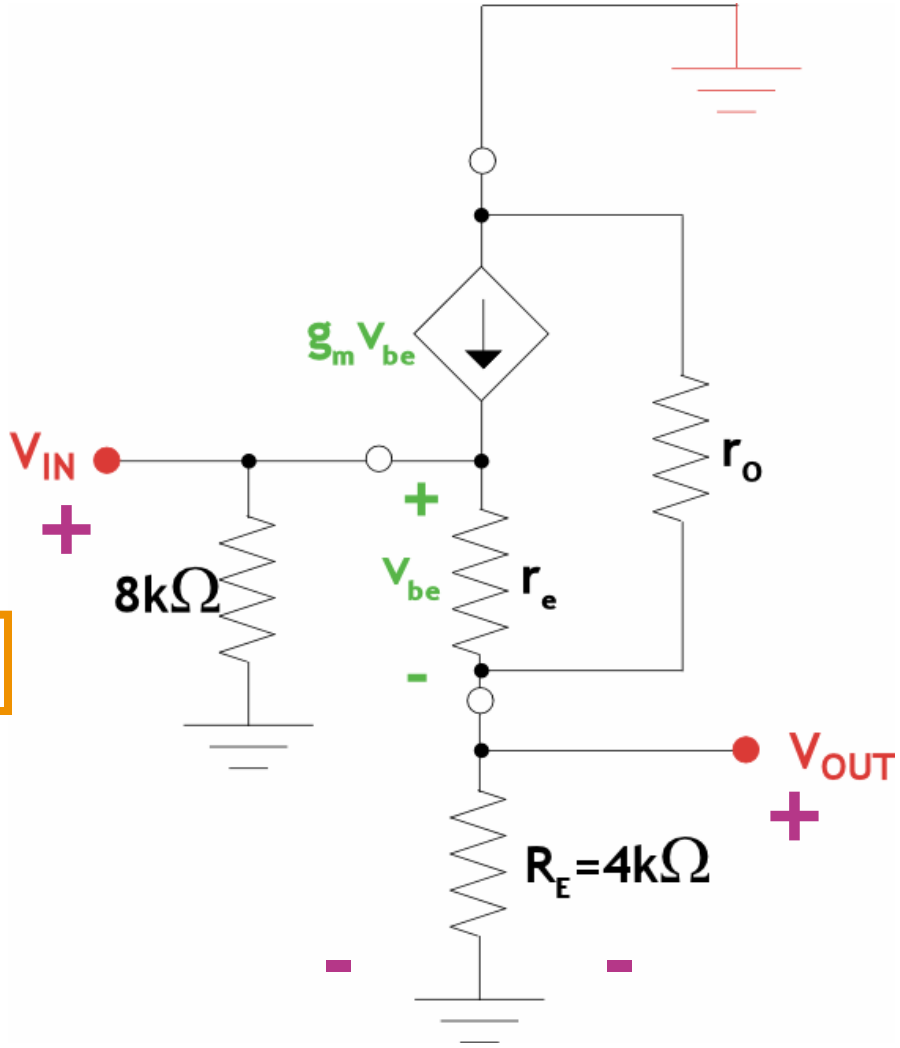
- Good voltage buffer
  - The VOLTAGE gain is almost unity, and the DC component is only reduced by 0.7V
  - Large short circuit current gain
  - High input resistance (which reduces loading to the circuits before)
  - Low output resistance (which reduces the loading to the circuits after)

CCA with r_o– Voltage-Gain Analysis

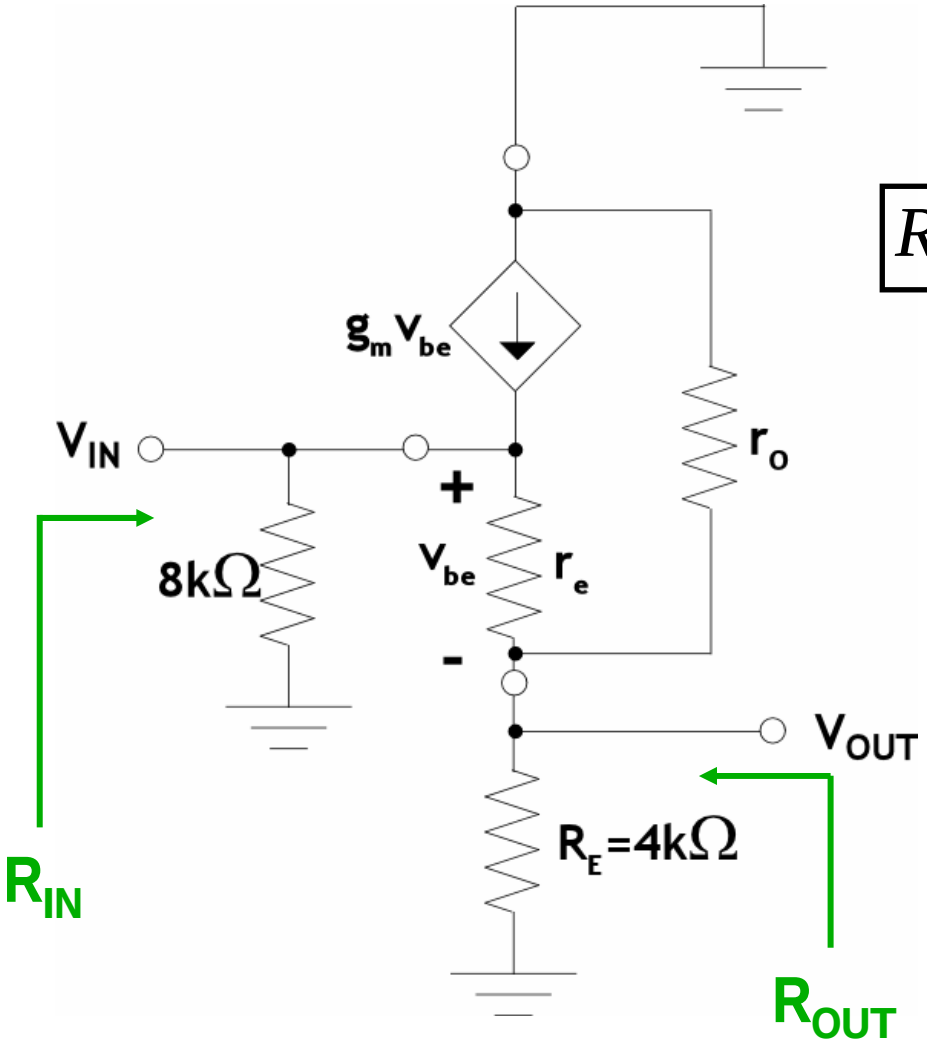
Voltage Division:

$$v_{out} = v_{in}\left(\frac{r_o \,//\, 4k\Omega}{r_o \,//\, 4k\Omega + r_e}\right)$$

Since r_e small, Almost $v_{out}=v_{in}$



CCA with r_o - Input/Output Resistance



- Input Resistance; by inspection using β+1 rule:

$$R_{IN} = 8k\Omega \,//\, \{(\beta+1)(r_e + r_o \,//\, R_E)\}$$

HIGH INPUT RESISTANCE

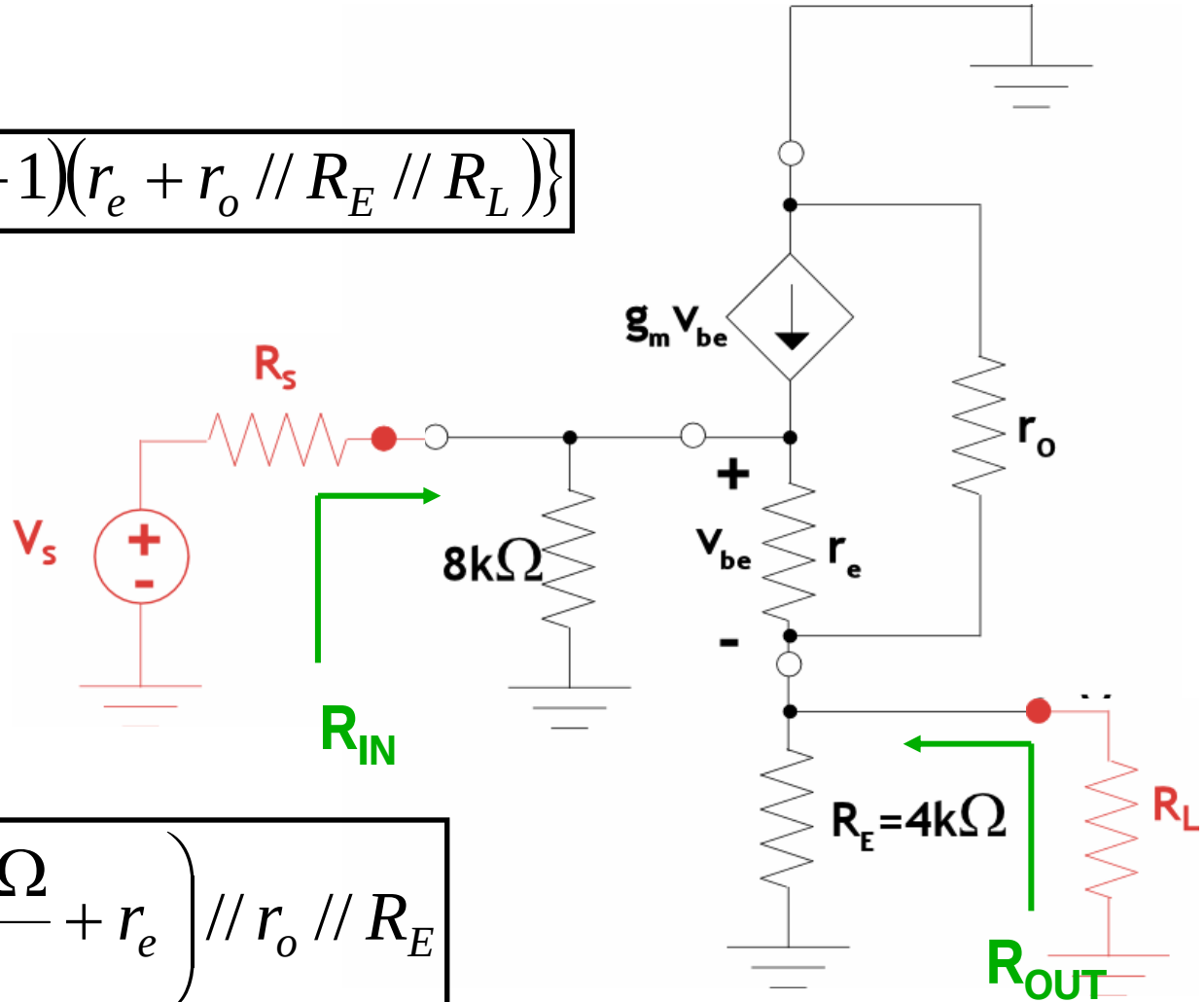
- Output Resistance, $v_{in} = 0$

$$R_{OUT} = r_e \,//\, r_o \,//\, R_E$$

LOW OUTPUT RESISTANCE

CCA with r_o , Source and Load

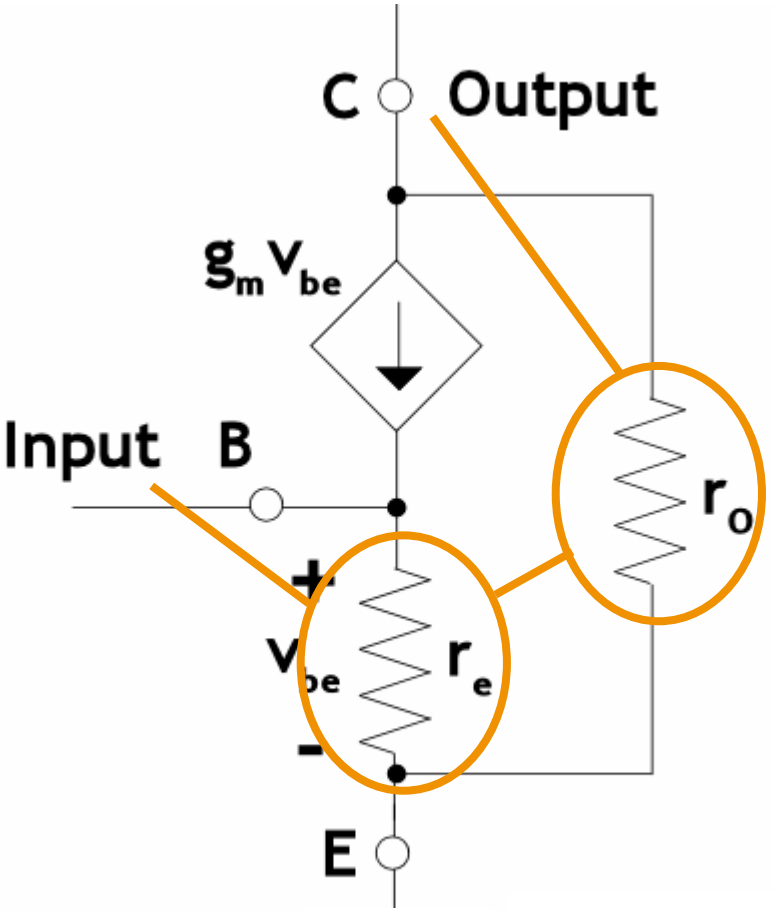
$$R_{IN} = 8k\Omega \,//\, \{(\beta+1)(r_e + r_o \,//\, R_E \,//\, R_L)\}$$



$$R_{OUT} = \left(\frac{R_S \,//\, 8k\Omega}{\beta+1} + r_e \right) // \, r_o \,//\, R_E$$

CEA with RE- Internal Feedback

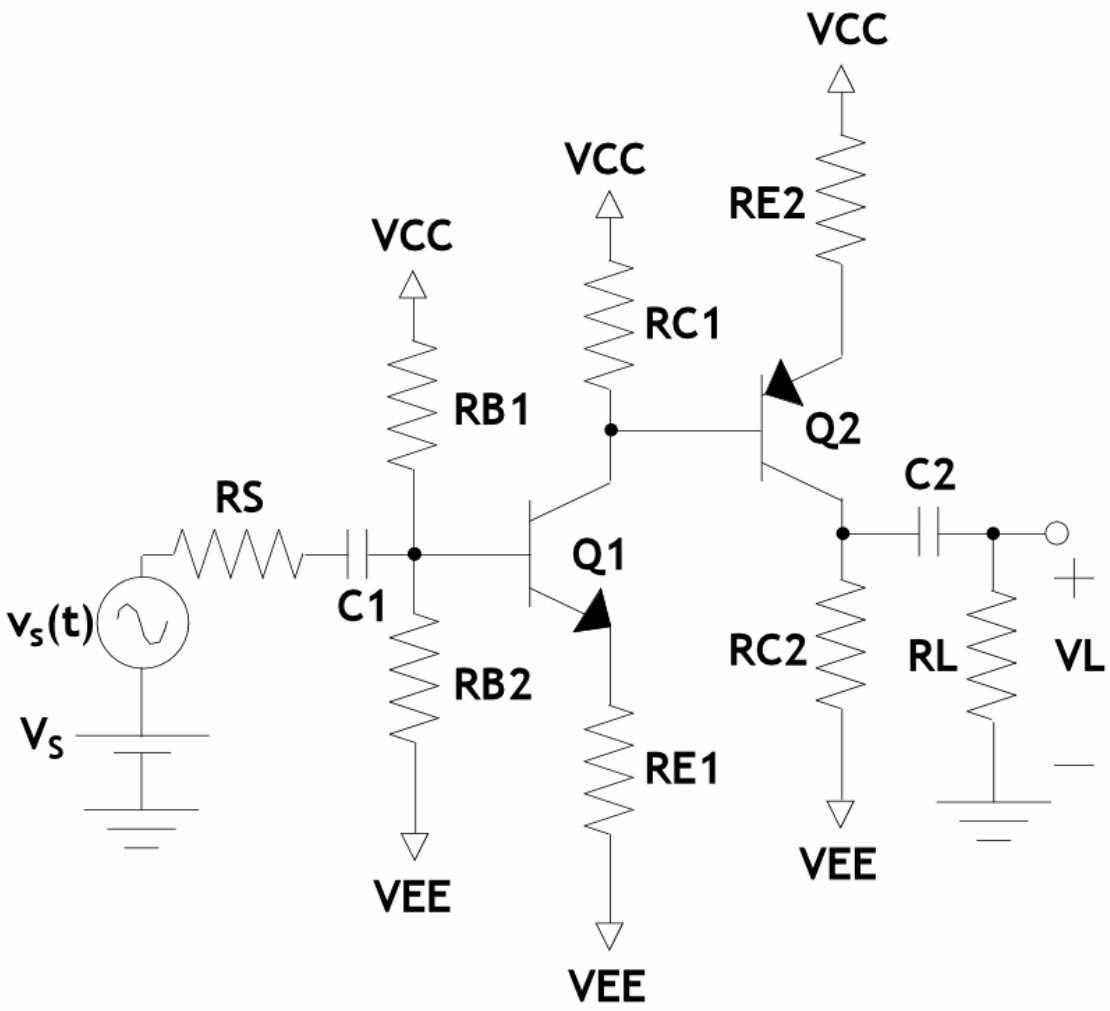
- Consider the small-signal T-model for the CEA configuration
- Base is input, collector is output
- r_e (or r_π – in Hybrid-π model) **AND** r_o both represent internal feedbacks from output to input; if emitter is grounded, feedback broken; if RE is present, feedback exists.



Internal Feedback – Summary

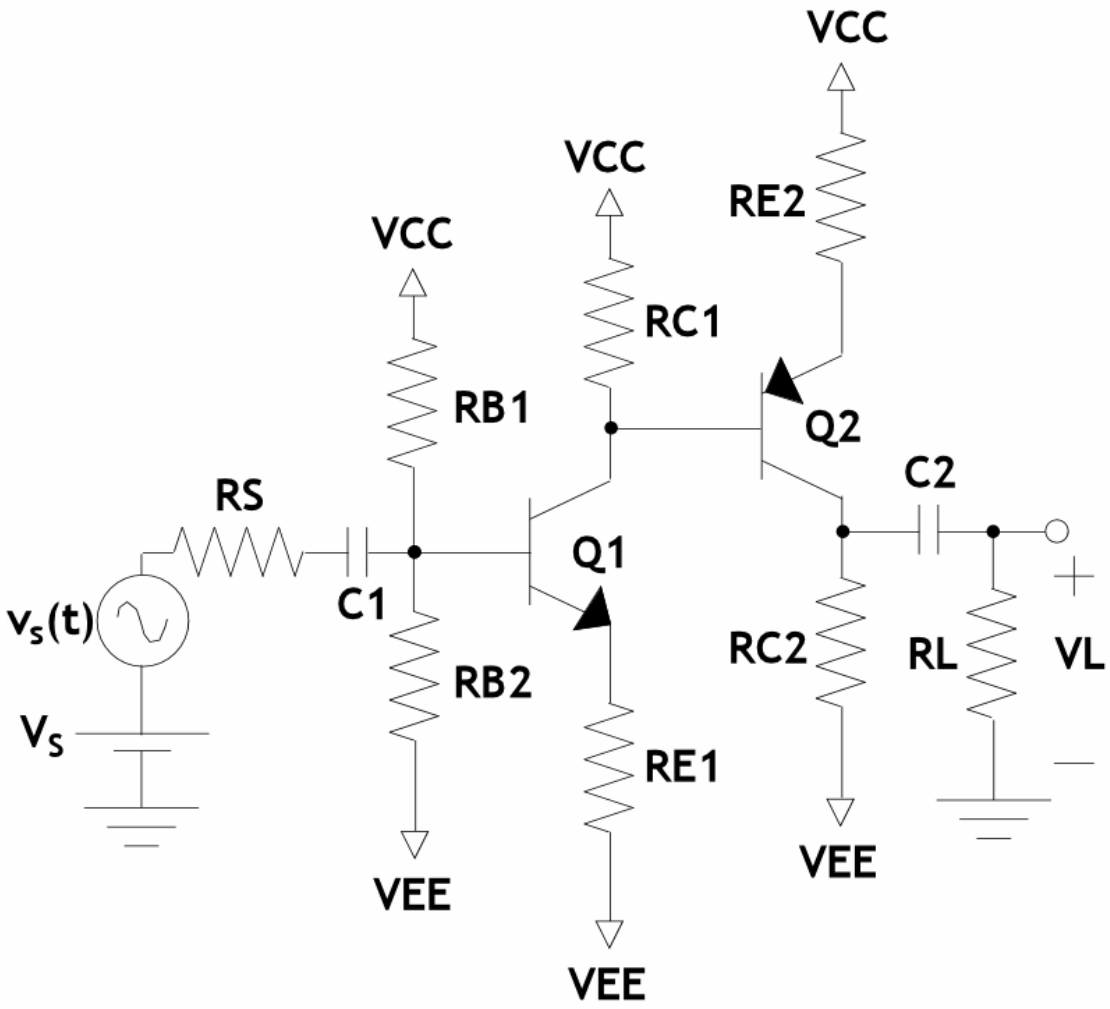
- CBA configuration:
  - r_o produces internal feedback between C & E terminals
  - expect effects to be ***weak*** since r_o large
- CCA configuration:
  - r_π or r_e produces internal feedback between B & E terminals
  - expect ***strong*** effect on R_{IN} & R_{OUT}
- CEA with R_E amplifier configuration:
  - r_o provides internal feedback between E & C terminals
  - occurs because emitter not at signal ground
  - expect ***weak*** effects since r_o large (More in EC2)
- CEA (no R_E) amplifier configuration:
  - no internal feedback between B & C terminals

Multistage Amplifier – DC Analysis



- Cascade of C-E stages
- Output of Q_1 stage is direct-coupled (DC) to input of Q_2 stage
- Coupled DC analysis!

Multistage Amplifier – R_{IN} & R_{OUT}



Find: R_{IN1}, R_{IN2}, R_{OUT1}, R_{OUT2}, A_{VO1}, A_{VO2}

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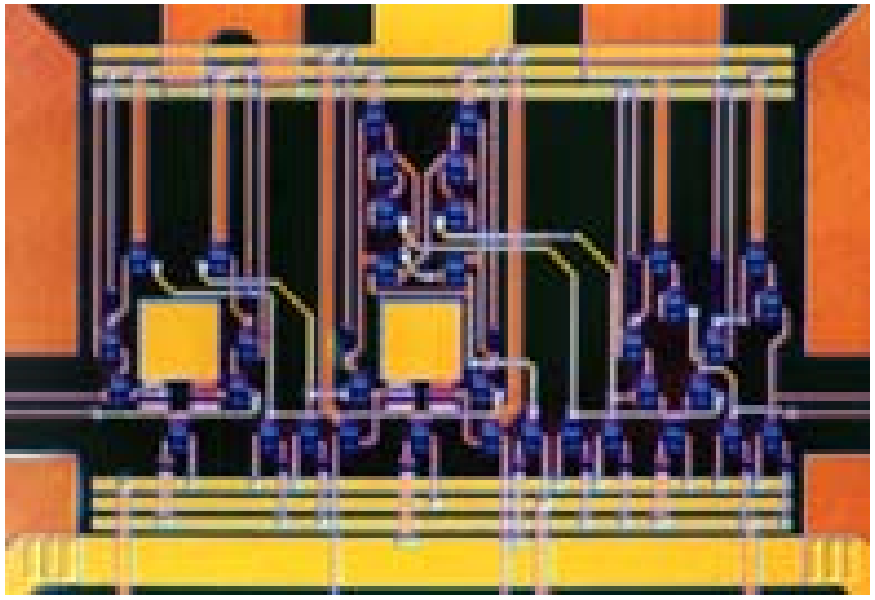
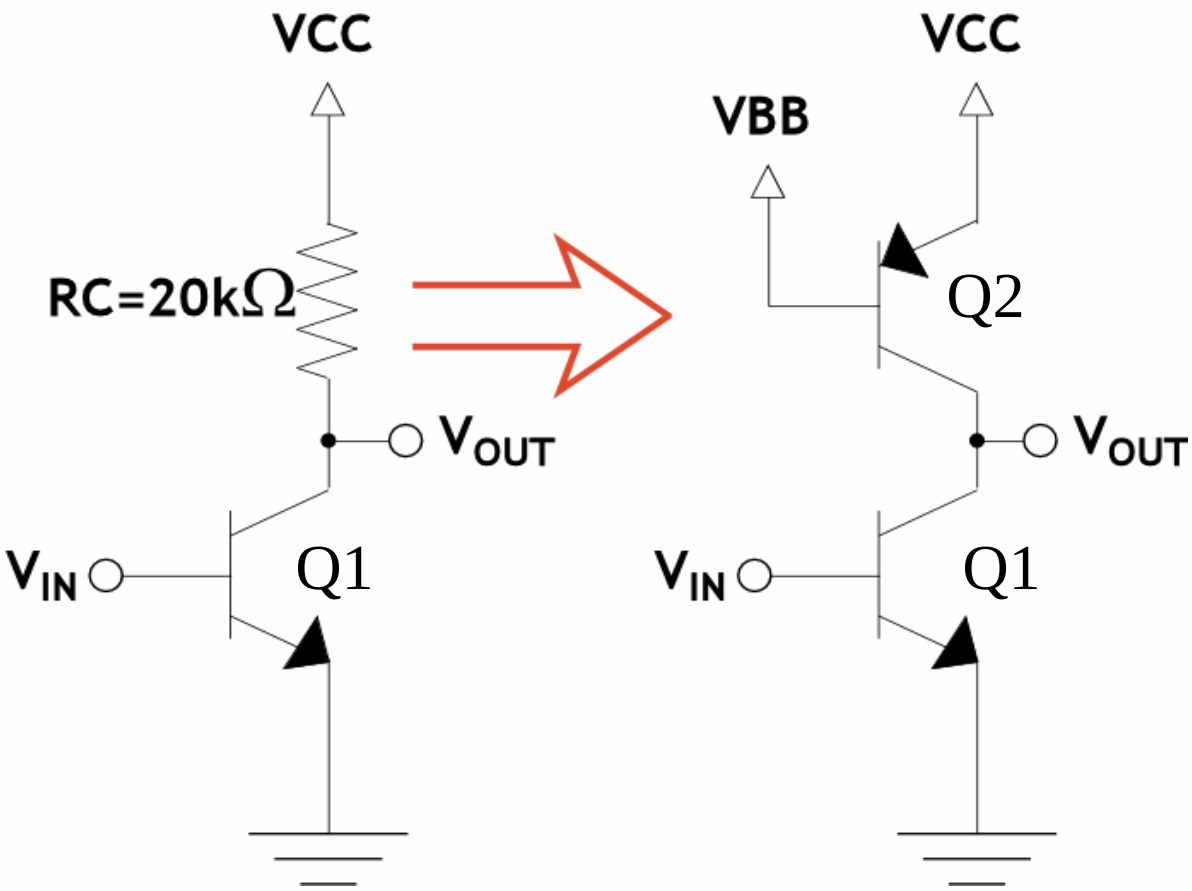
Integrated Circuits



- Issues:
  - Limited area available
  - Size of R's and C's limited
  - Process variations

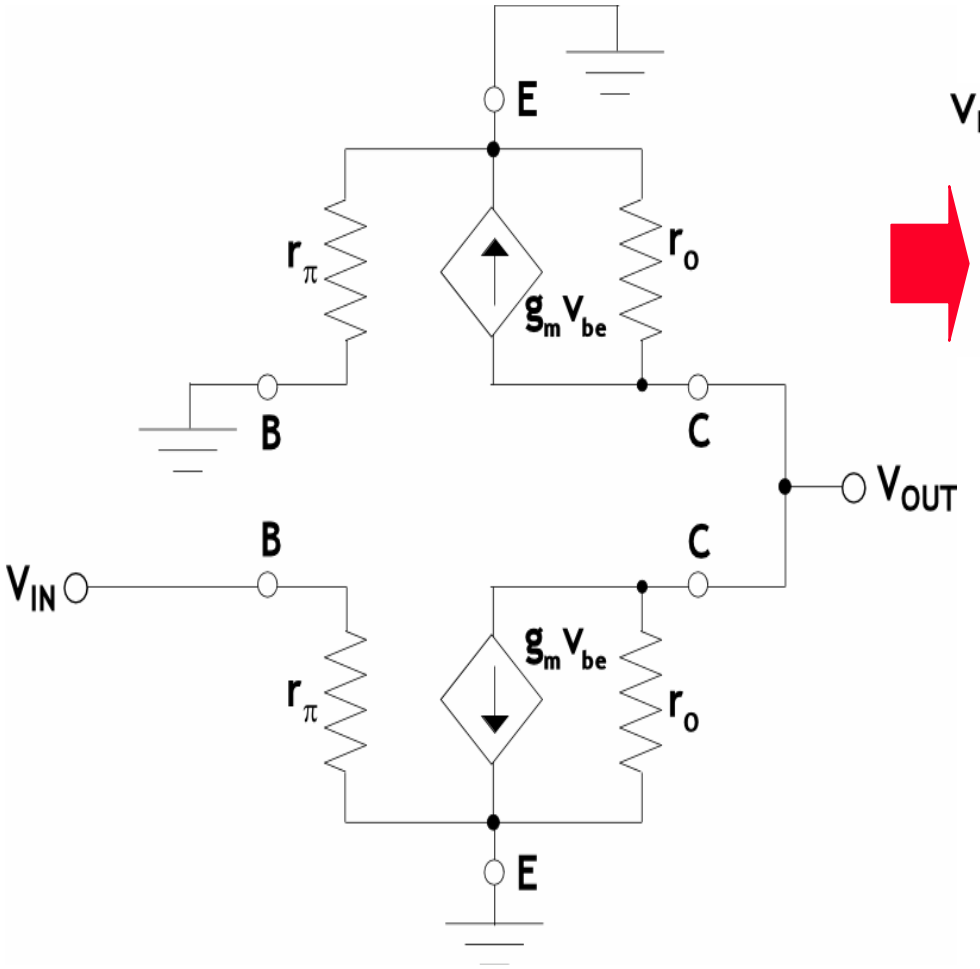
- Concept:
  - Integrate multiple transistors and passive components (R's and C's) on a single chip
  - Circuit performs application-specific function (ASIC)
  - Physically smaller, faster
- Coupling capacitors:
  - On-chip: ~ pF's only
  - Off-chip: ~ μF's
- Resistors:
  - Pure resistors are difficult to make on an IC
  - Alternative: a transistor

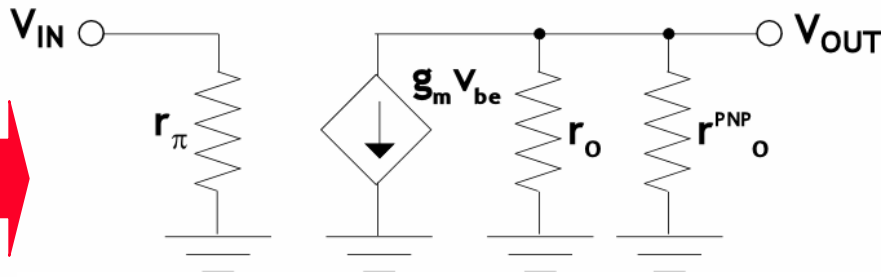
Active Loads



- Replace R_C with PNP transistor, Q2
- Q2 base held at constant voltage.
- Q1 load resistance becomes r_o of Q2.

CEA Gain with Active Load





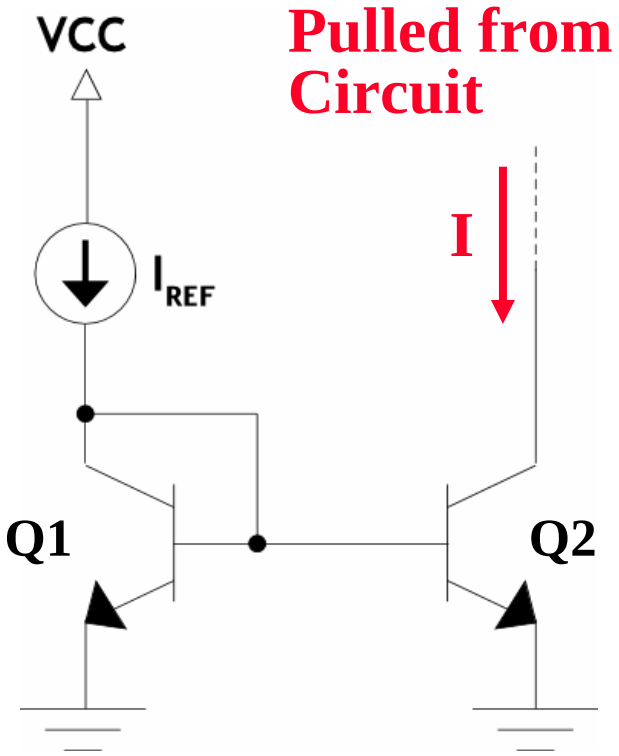
$$A_V = -g_m \cdot \left(r_{o1} \| r_{o2}\right)$$

$$g_m = \frac{I_C}{V_T} \qquad r_o = \frac{V_A}{I_C}$$

$$\boxed{A_V = -\frac{V_A}{2 \cdot V_T}}$$

Current Mirrors

- CBA and CCA conveniently biased with current sources
- On an IC, a current source is implemented using transistors
- I_{REF} can be implemented off-chip, resistor
- Transistor Q2 pulls current from attached circuit
- Collector current of Q1 and Q2 identical because of V_{BE} is the same (r_o neglected)

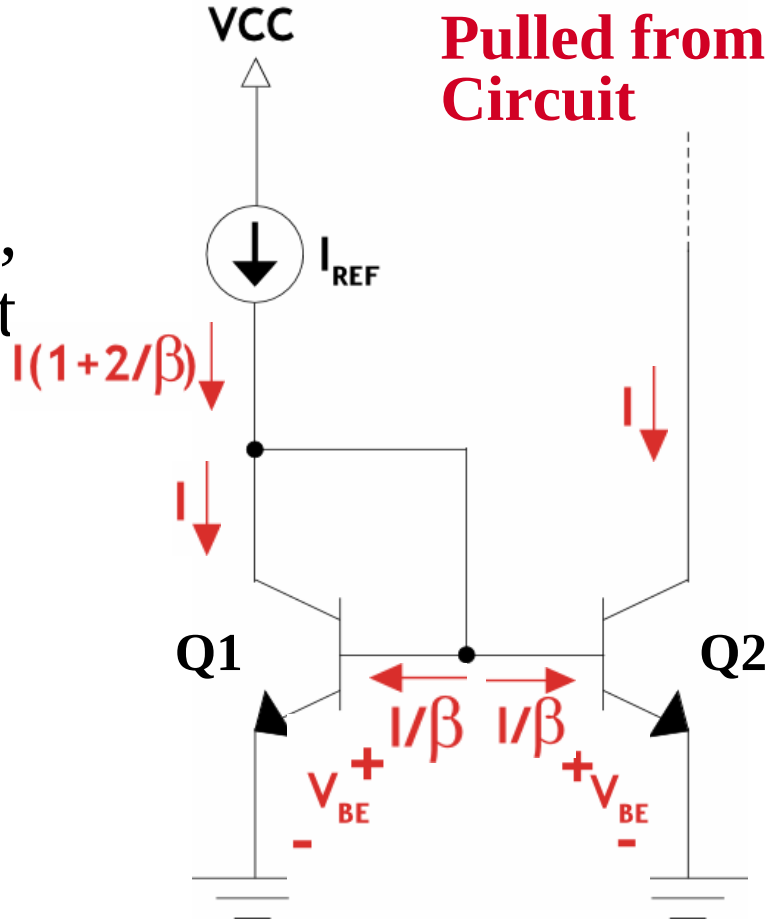


Current Mirror DC Analysis

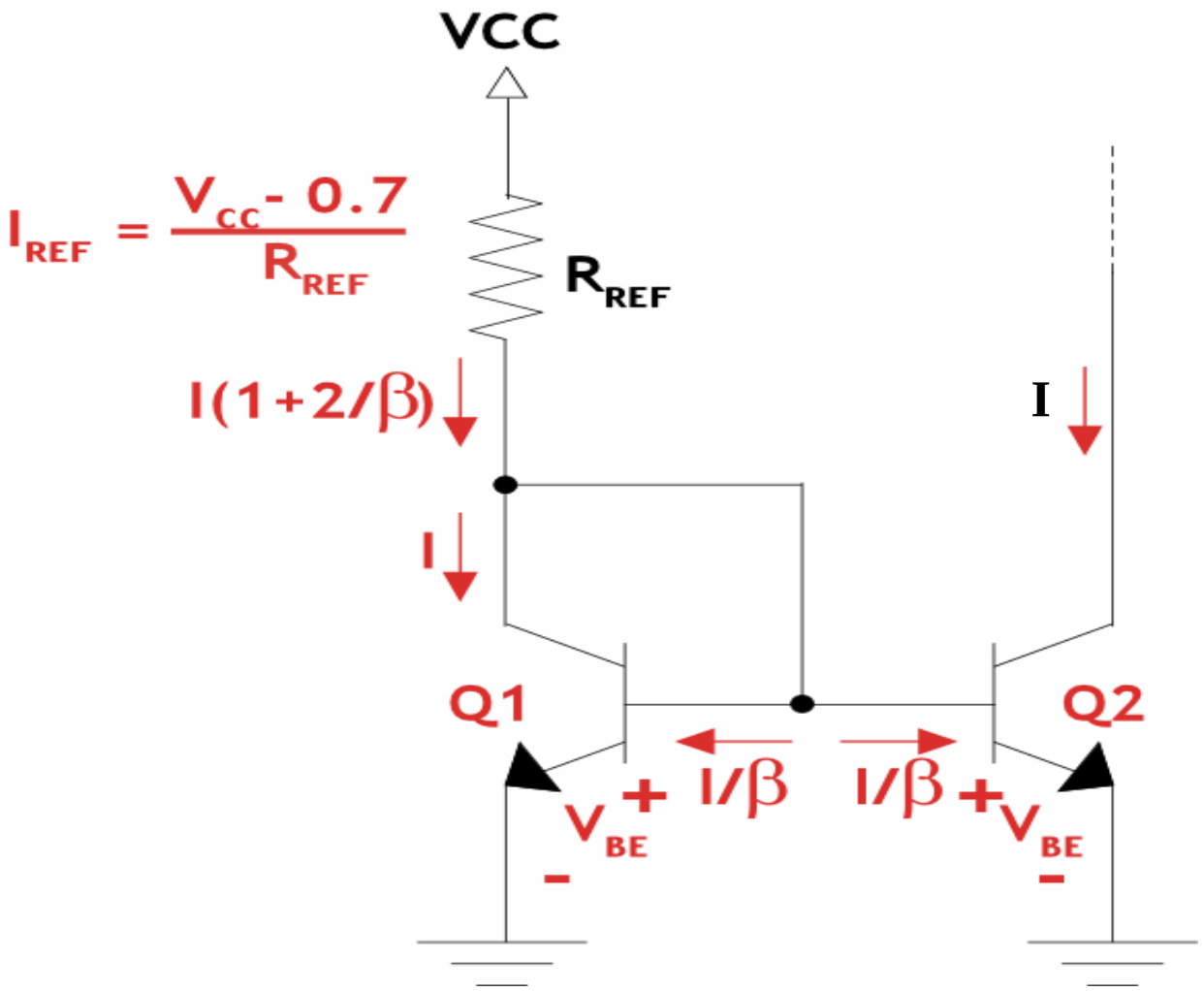
- Neglect r_o (in EC1 DC analysis) and assume Q1 and Q2 active
- If Q1 has a collector current of I, then there must be a base current of I/β.
- This sets-up a Q1 V_{BE1} that is "mirrored" across to the base emitter of Q2, V_{BE2}.
- V_{BE2} draws a current of I from the Q2 collector.

$$I_{REF} = I + 2\frac{I}{\beta}$$

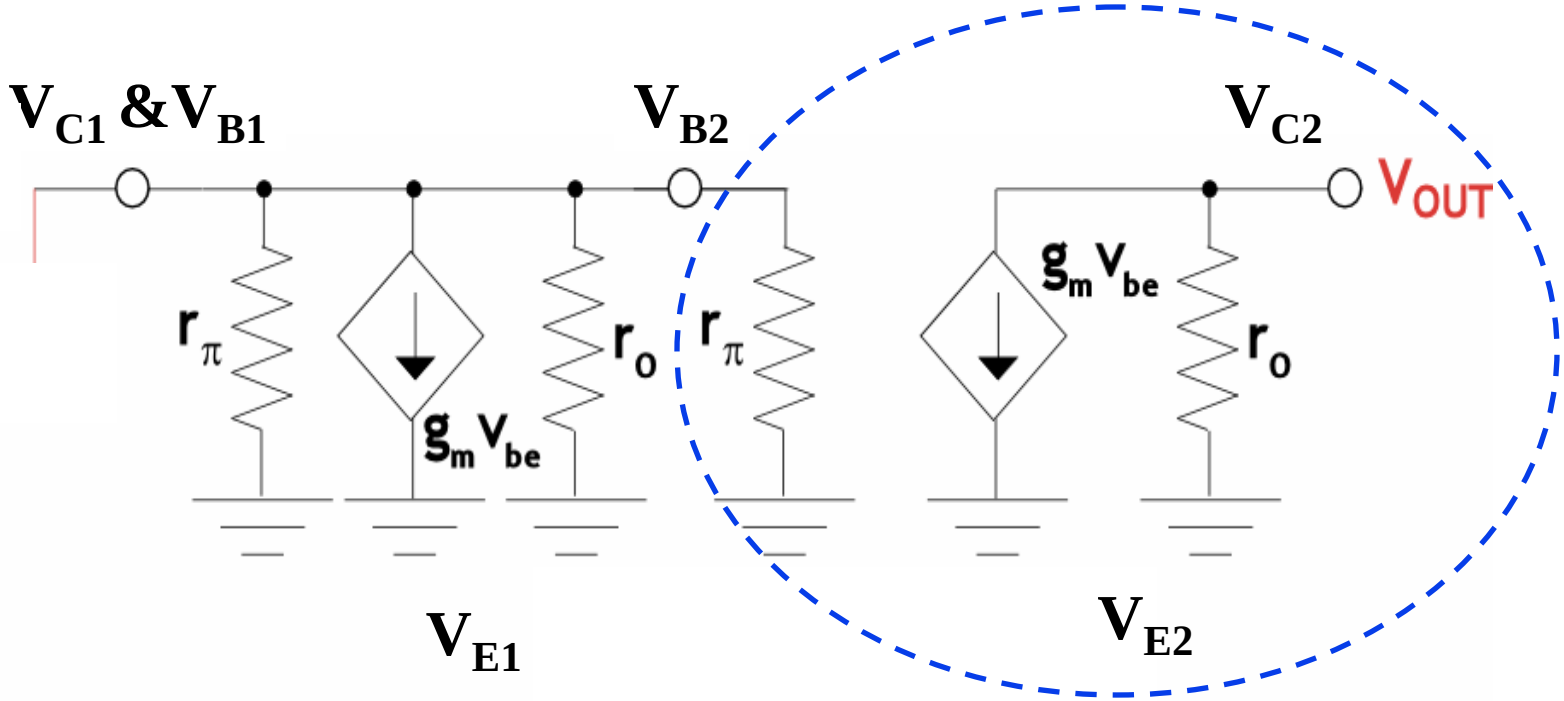
$$\frac{I}{I_{REF}} = \frac{1}{1+\frac{2}{\beta}}$$



Current Mirror DC Analysis



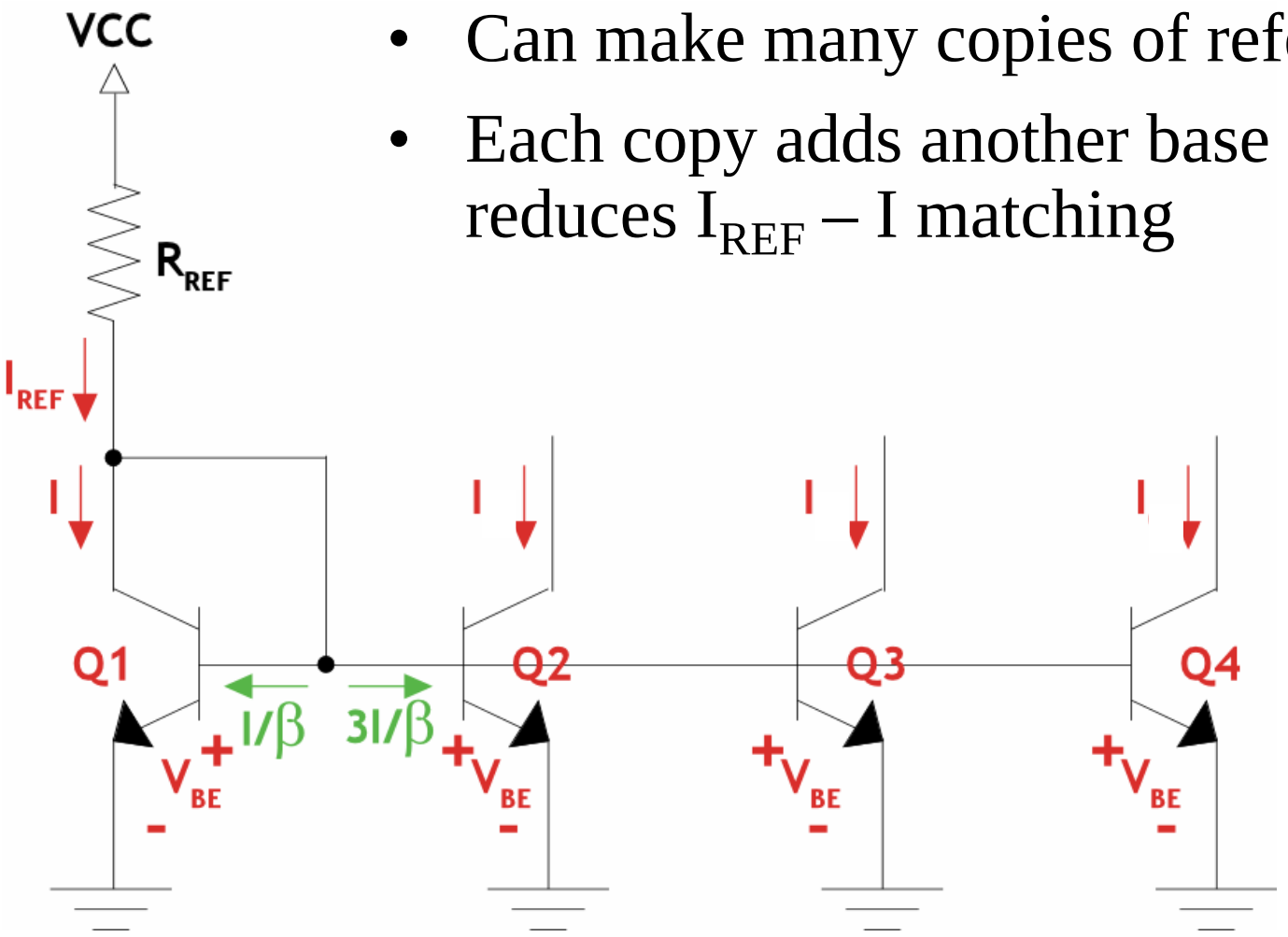
Current Mirror AC Analysis



Impact of current mirror is to add a load r_o to circuit that is drawing current

Note: In AC analysis r_o is included

Current Mirroring – Multiple Copies

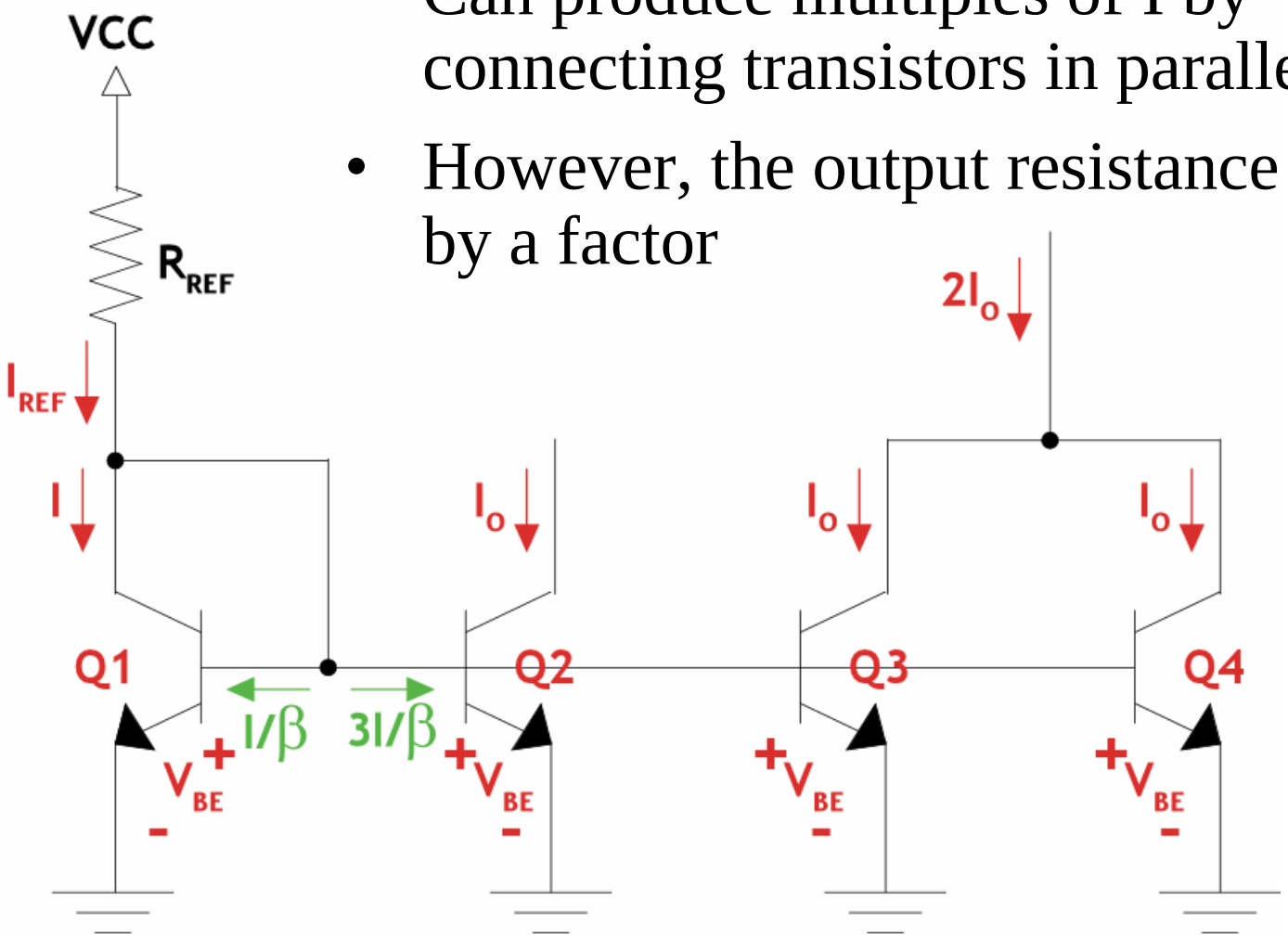


- Can make many copies of reference current
- Each copy adds another base current draw, reduces I_{REF} – I matching

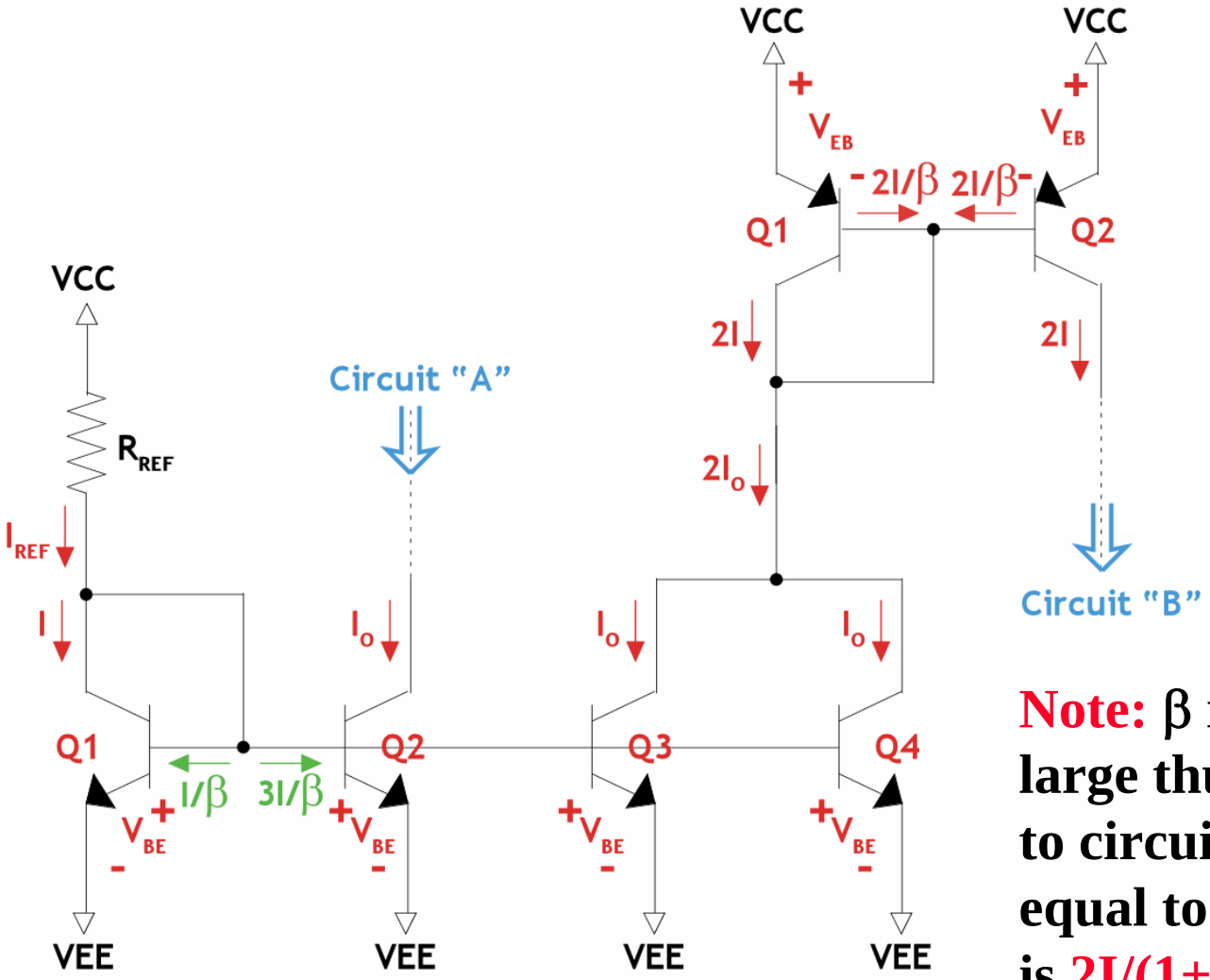
$$\frac{I}{I_{REF}} = \frac{1}{1+\frac{N+1}{\beta}}$$

Current Mirroring – Scaling

- Can produce multiples of I by connecting transistors in parallel
- However, the output resistance is decreased by a factor



Current Mirroring – Pushing and Pulling

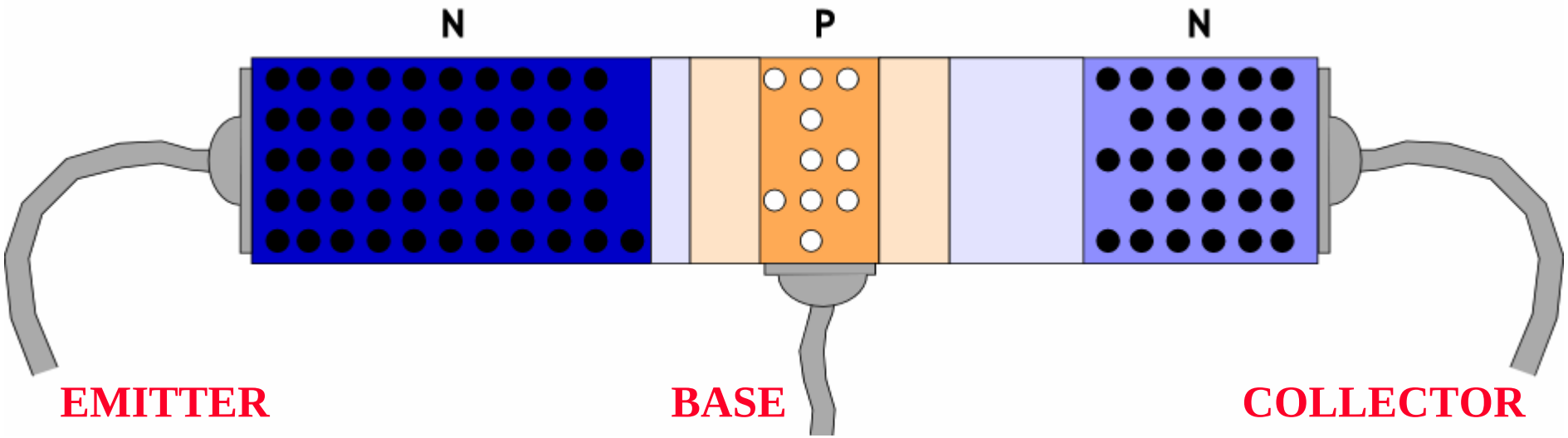


Note: β **is assumed to be very large thus the current pushed to circuit B is approximated equal to 2I. The exact answer is** $2I/(1+2/\beta)$

Outline of Chapter 5

- 1- Cut-off and Saturation Modes
- 2- Digital Circuits

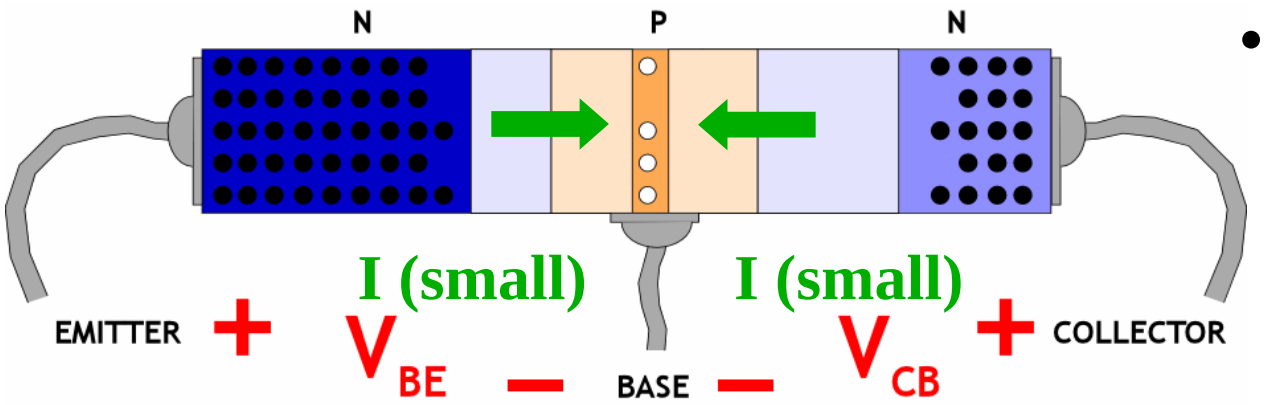
The npn BJT Operational Modes



4 Modes of operation

	B-E Junction	B-C Junction
Cutoff	reverse	reverse
Active	forward	reverse
Saturation	forward	forward
Reverse Active	reverse	forward

Cutoff Mode



- Reverse-bias drift currents are ***SMALL***

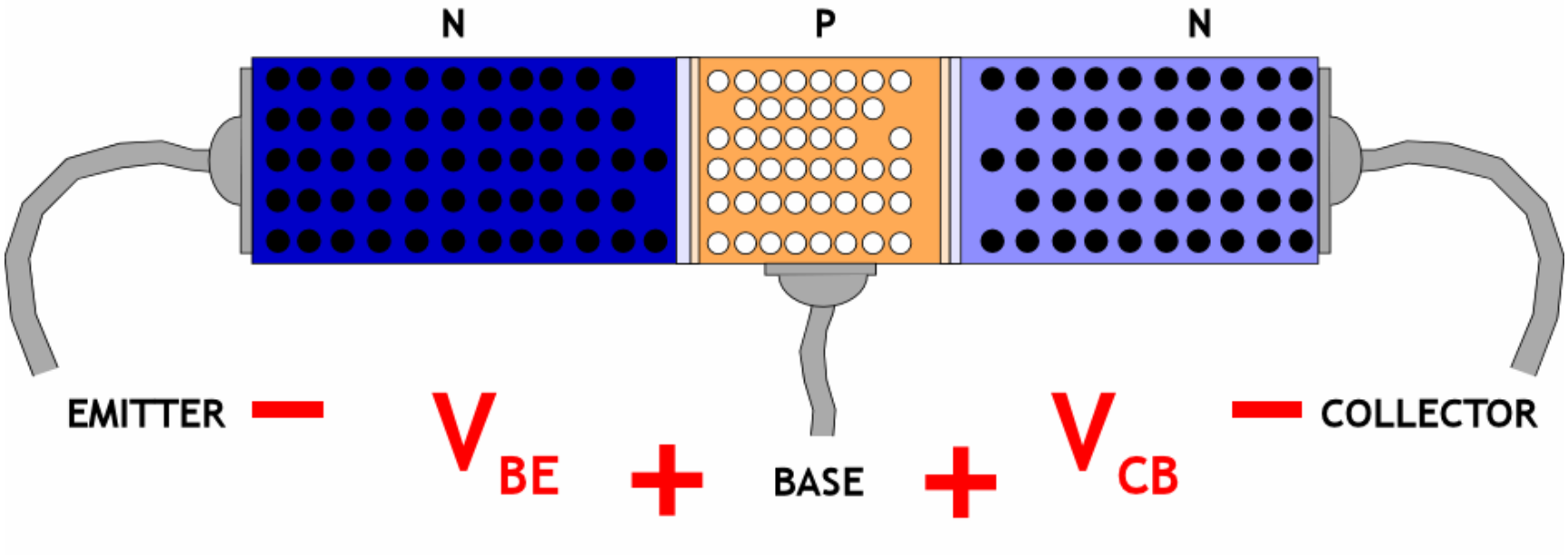
- Cutoff mode:
  - B-E pn junction reverse-biased
  - B-C pn junction reverse-biased

- Drift currents:
  - From E to B
  - From C to B

4 Modes of operation

	B-E Junction	B-C Junction
Cutoff	reverse	reverse
Active	forward	reverse
Saturation	forward	forward
Reverse Active	reverse	forward

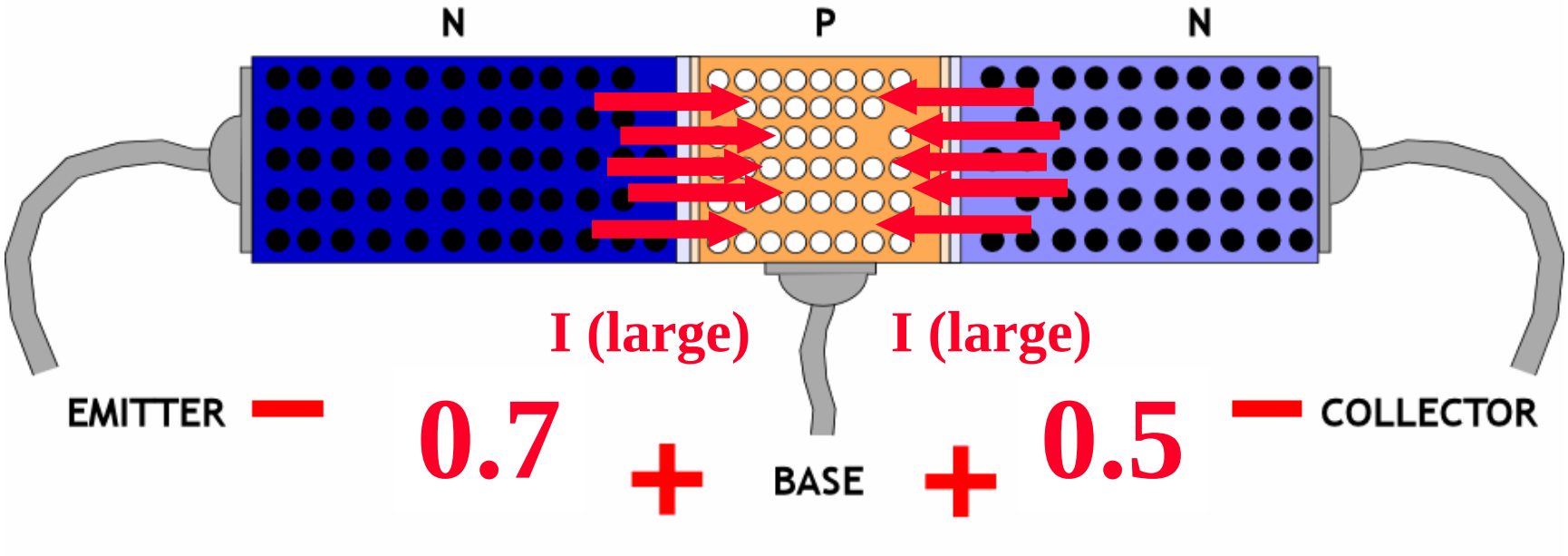
Saturation Mode



4 Modes of operation

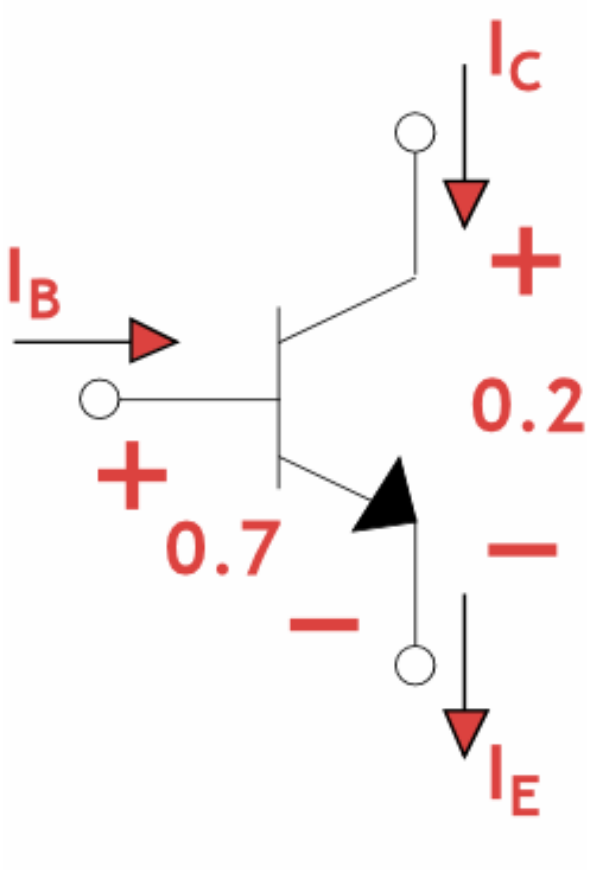
	B-E Junction	B-C Junction
Cutoff	reverse	reverse
Active	forward	reverse
Saturation	forward	forward
Reverse Active	reverse	forward

Saturation Mode – Operation (1)



- Saturation mode:
  - B-E pn junction forward-biased
  - B-C pn junction forward-biased
- Electron diffusion current from E to B
  - Base recombination
  - Traverses base into collector
- Electron diffusion current from C to B
  - Base recombination
  - Traverses base into emitter

Saturation Mode – I_C, I_B, and I_E



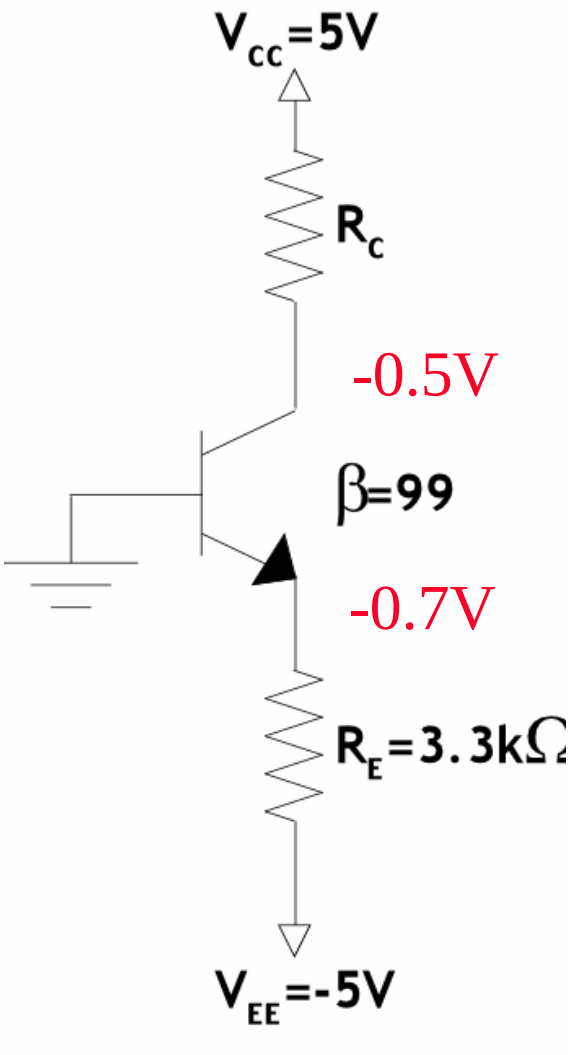
- β (and α) as we know it only applies in active mode
- "new" β (β_{forced}) set by external components

$$V_{CE-SAT} = 0.2V$$

$$I_E = I_C + I_B$$

$$\beta_{forced} = \frac{I_C}{I_B}$$

Saturation DC Analysis



- For $R_C = 5k\Omega$, BJT enters saturation
- Apply voltage drop criteria, solve for currents

$$I_E = \frac{-0.7+5}{3.3k} = 1.303mA$$

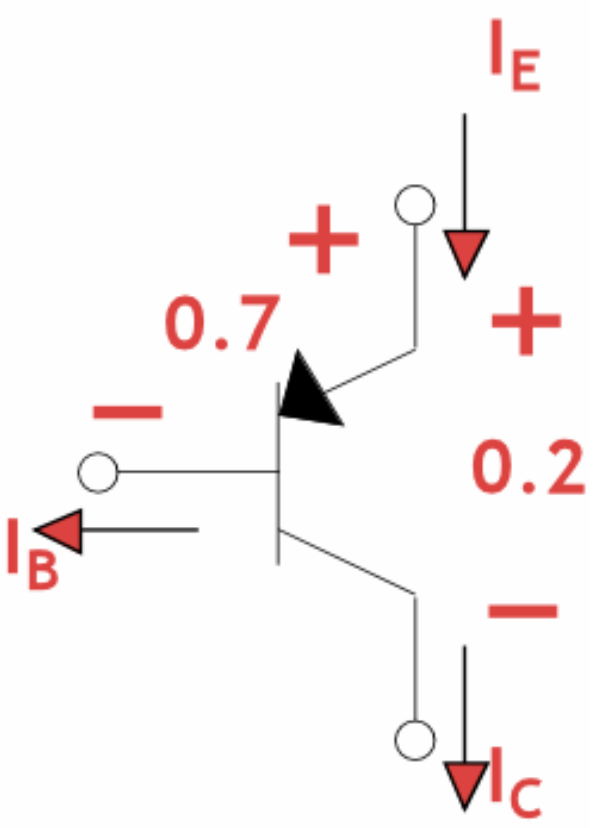
$$I_C = \frac{5+0.5}{5k} = 1.1mA$$

$$I_B = I_E - I_C = 203\mu A$$

$$\beta_{forced} = \frac{I_C}{I_B} = \frac{1.1m}{203\mu} = 5.4 << \beta$$

Comments

- $\beta_{forced} << \beta$ in saturation
- Current directions (I_C, I_B, I_E) same as for active mode
- All concepts & expressions same for **PNP** in saturation



$$V_{EC-SAT} = 0.2V$$

$$I_E = I_C + I_B$$

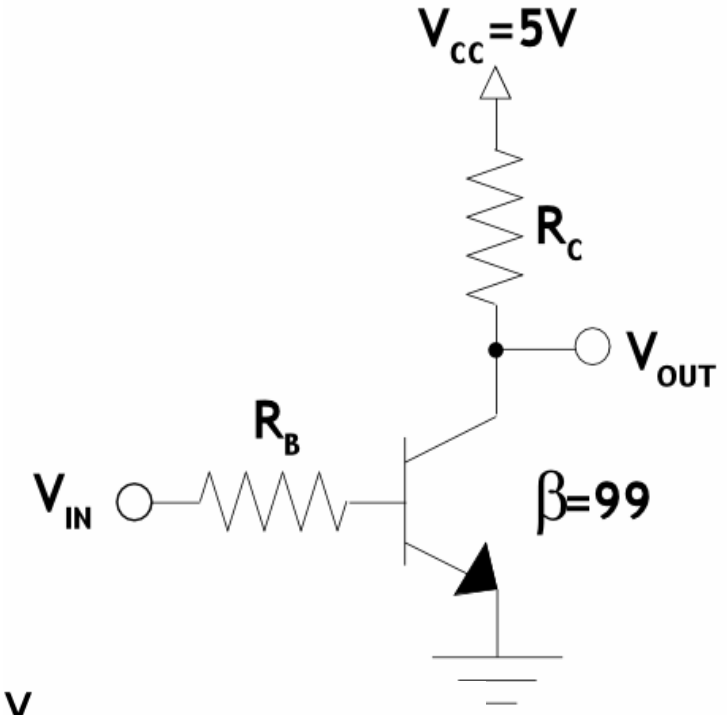
$$\beta_{forced} = \frac{I_C}{I_B}$$

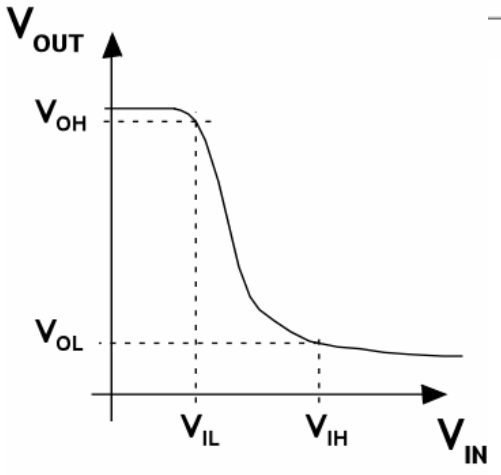
CEA as an Inverter

- The large negative voltage gain of the CEA was:

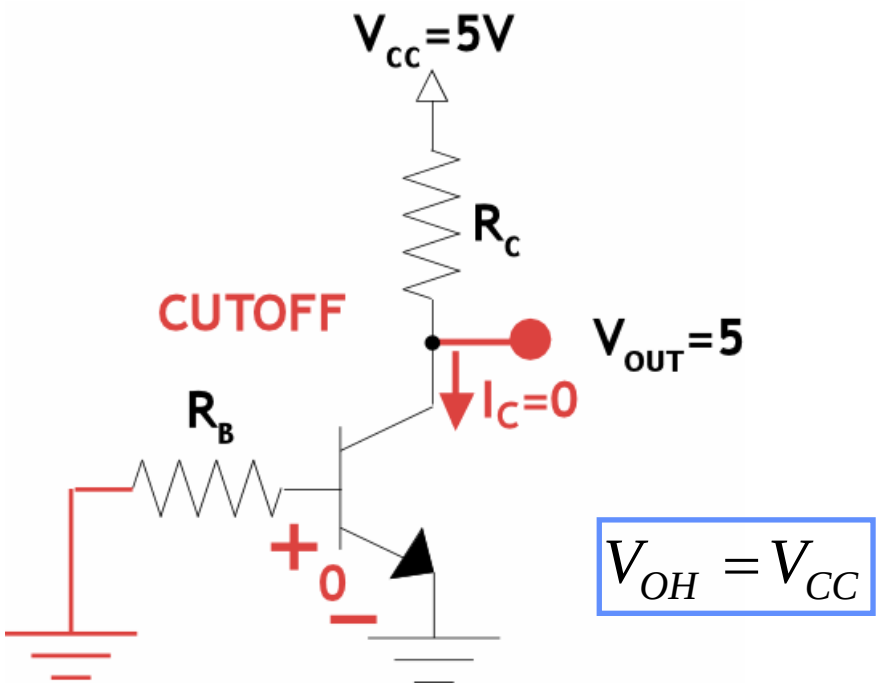
$$A_{VO} = \frac{v_{out}}{v_{be}} = -g_m\left(r_o \| R_C\right)$$

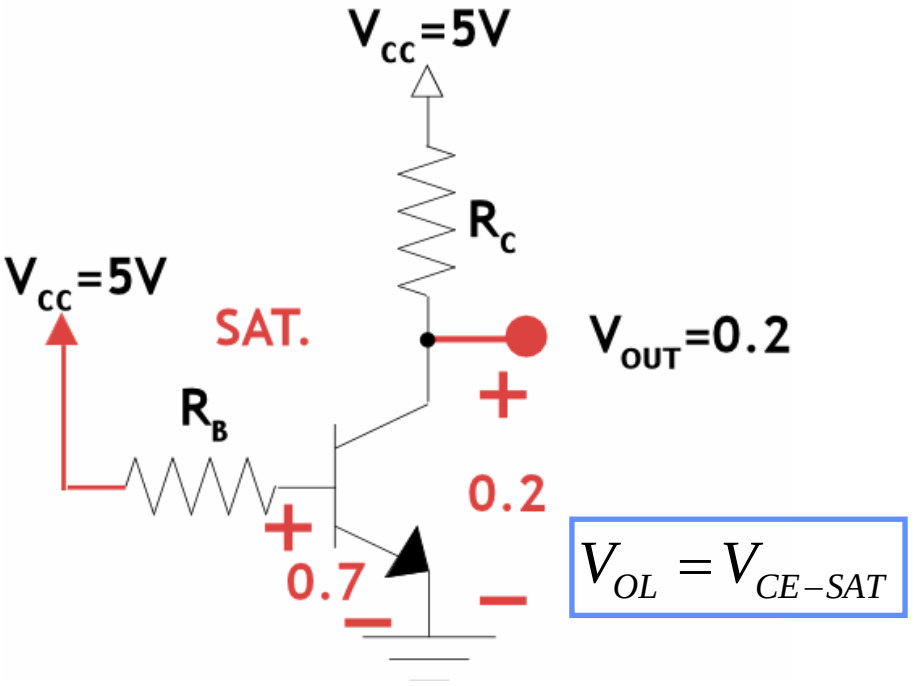
- This produces a sharp linear region that describes Vout/Vin for device in active-mode.
- Max. output (cut-off) and min. output (saturation).
- Through analysis, we can describe the Voltage Transfer Characteristic (VTC)





CEA Inverter





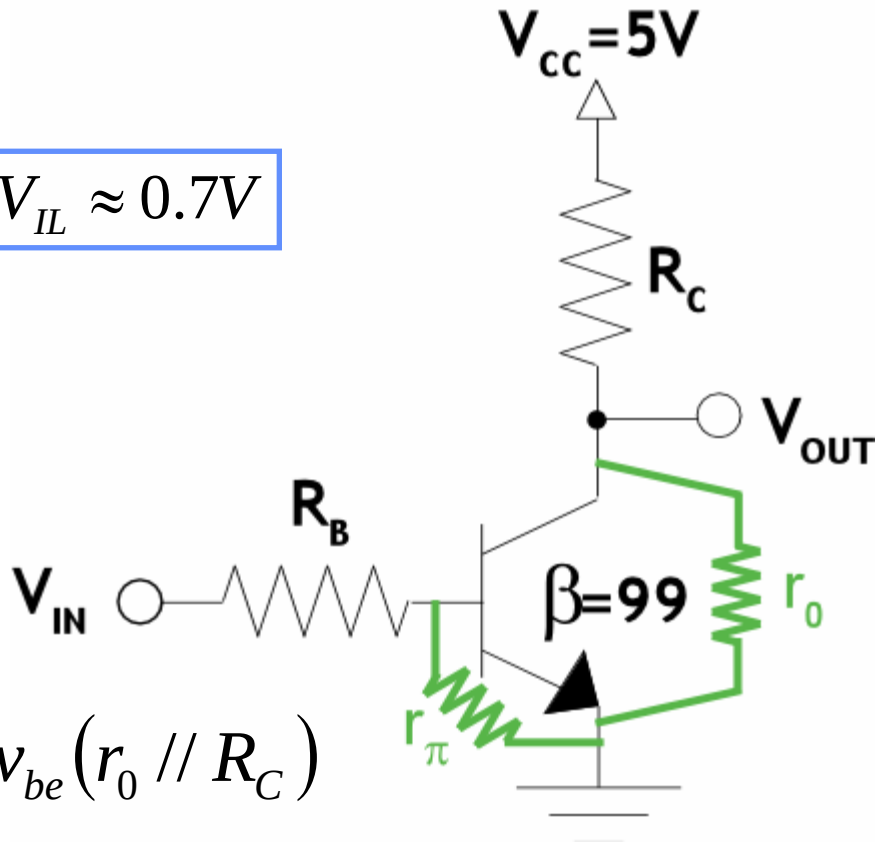
- When V_{IN} = 0
  - BJT is in cutoff
  - I_C = 0
  - V_{OUT} = VCC

- When V_{IN} = 5
  - BJT is in saturation
  - V_{OUT} = 0.2

CEA Inverter - V_{IL}

- BJT remains in cutoff until $V_{IN} \approx 0.7V$, then enters active mode because B-E junction goes into FWD bias
- As V_{IN} rises in active mode, V_{OUT} decreases

$$V_{IL} \approx 0.7V$$

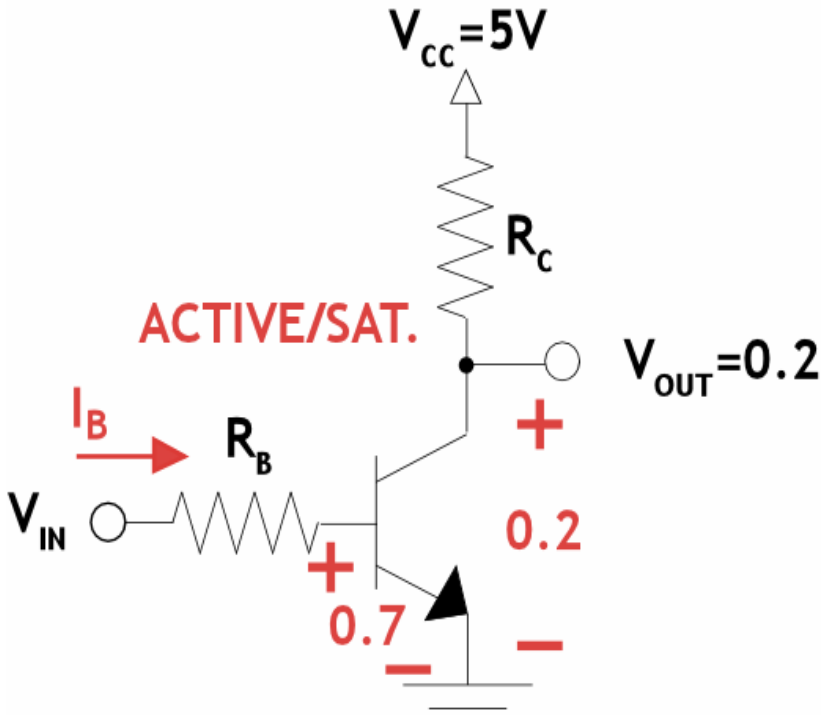


$$v_{be} = \frac{r_\pi}{r_\pi + R_B} v_{IN} \qquad v_{OUT} = -g_m v_{be} (r_0 \,//\, R_C)$$

$$A_V = \frac{v_{OUT}}{v_{IN}} = \frac{-g_m r_\pi}{r_\pi + R_B}(r_0 \,//\, R_C) = \frac{-\beta}{r_\pi + R_B}(r_0 \,//\, R_C)$$

CEA Inverter - V_{IH}

- To find V_{IH}:
  - Must use the "Edge-of-Saturation" (EOS)
  - The Max. I_B at the threshold of Active/Sat. defined as $I_{B\text{-}EOS}$



$$V_{IN} = 0.7 + I_B R_B$$

$$I_{B-EOS} = \frac{I_{C-SAT}}{\beta} = \frac{V_{CC} - V_{CE-SAT}}{\beta R_C}$$

$$V_{IH} = 0.7 + I_{B-EOS} R_B = 0.7 + \frac{V_{CC} - V_{CE-SAT}}{\beta R_C} R_B$$

CEA Inverter Voltage Transfer Characteristic (VTC)

Consider V_{CC}=5V, R_B=10kΩ, R_C=1kΩ, β=100, V_A=100V

Hand-analysis:

$V_{IL} \approx 0.7V$ $V_{OL} \approx 0.2V$

$V_{OH} = 5V$ $V_{IH} = 1.18V$

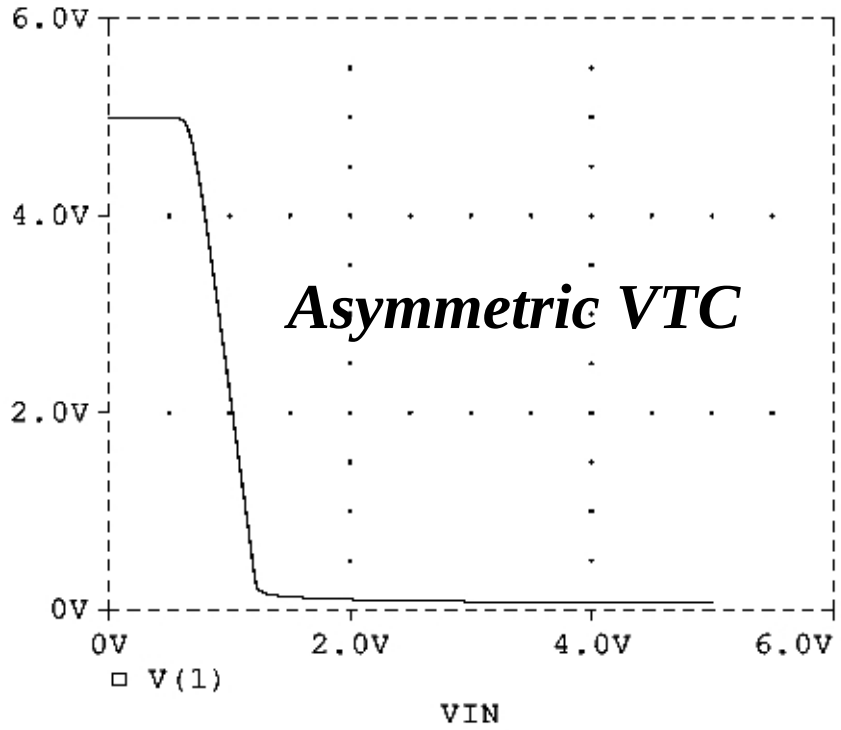
Noise margins:

$$NM_H = V_{OH} - V_{IH} = VCC - 0.7V - I_{B-EOS} R_B$$

$$NM_L = V_{IL} - V_{OL} = 0.7V - V_{CE-SAT} = 0.5V$$

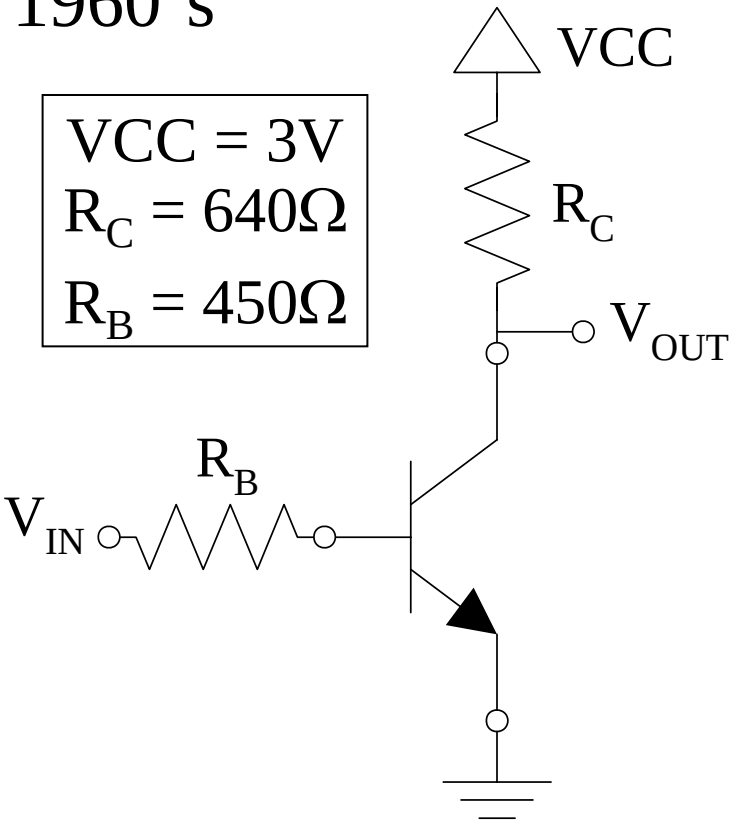
$NM_H = 3.82V$ $NM_L = 0.5V$

VTC (simulation)



Resistor-Transistor Logic (RTL) Inverter

- Popular technology in 1960's



- Using equations:

$V_{IL} \approx 0.7V$ $V_{OL} \approx 0.2V$

$V_{OH} = 3V$ $V_{IH} = 0.72V$

$NM_H = 2.28V$ $NM_L = 0.5V$

More in EC2