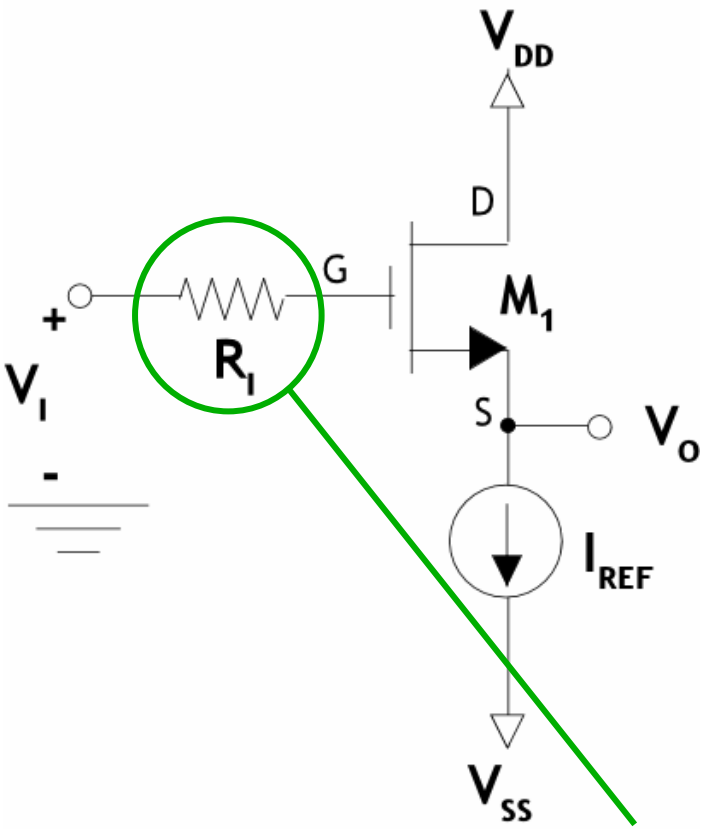
Outline of Chapter 4

- 1- Intro to MOS Field Effect Transistor (MOSFET)
- 2- NMOS FET
- 3- PMOS FET
- 4- DC Analysis of MOSFET Circuits
- 5- MOSFET Amplifier
- 6- MOSFET Small Signal Model
- 7- MOSFET Integrated Circuits
- 8- CSA, CGA, CDA
- 9- CMOS Inverter & MOS Digital Logic

Common Drain Amplifier (CDA)



- A nMOS current mirror is used as I_{REF} including the output resistance.
- Voltage signal source DC-coupled to gate terminal
- Drain terminal held at a DC voltage
- Since source terminal not at signal ground, Body effect exists

R_I is the resistance from previous stage

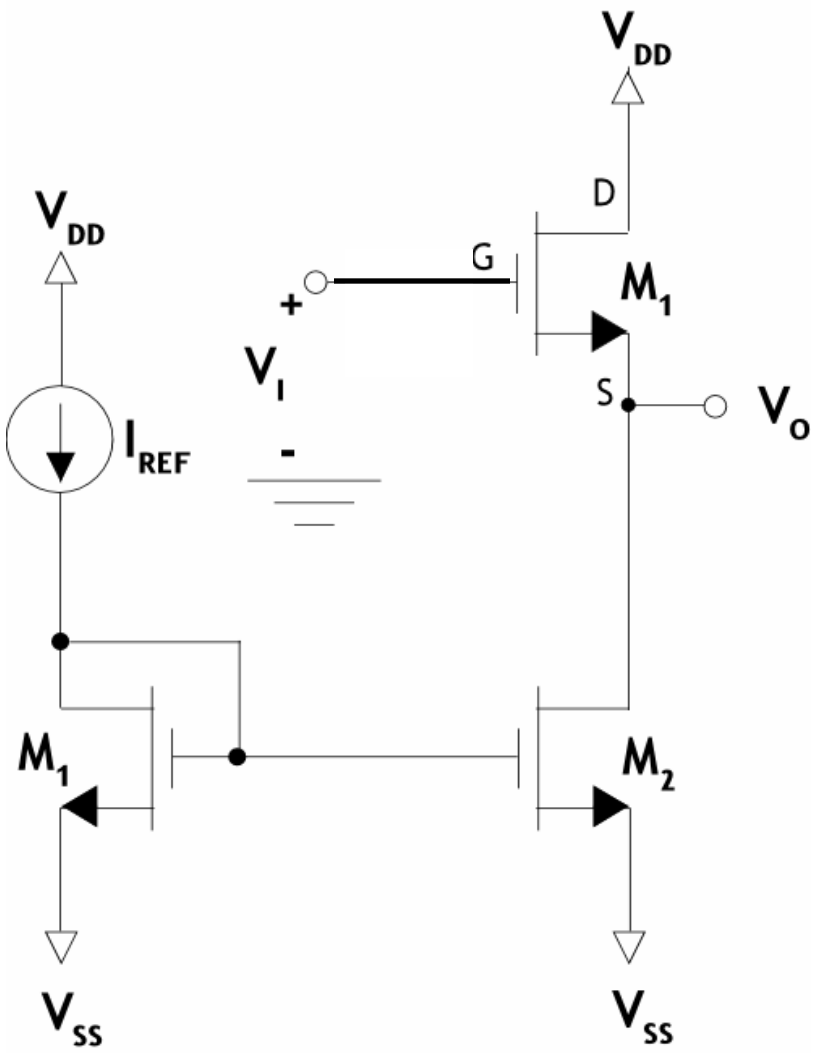
CDA

- Replace with a “real” current source including output resistance r_{o2}
- No problem including AC CLM

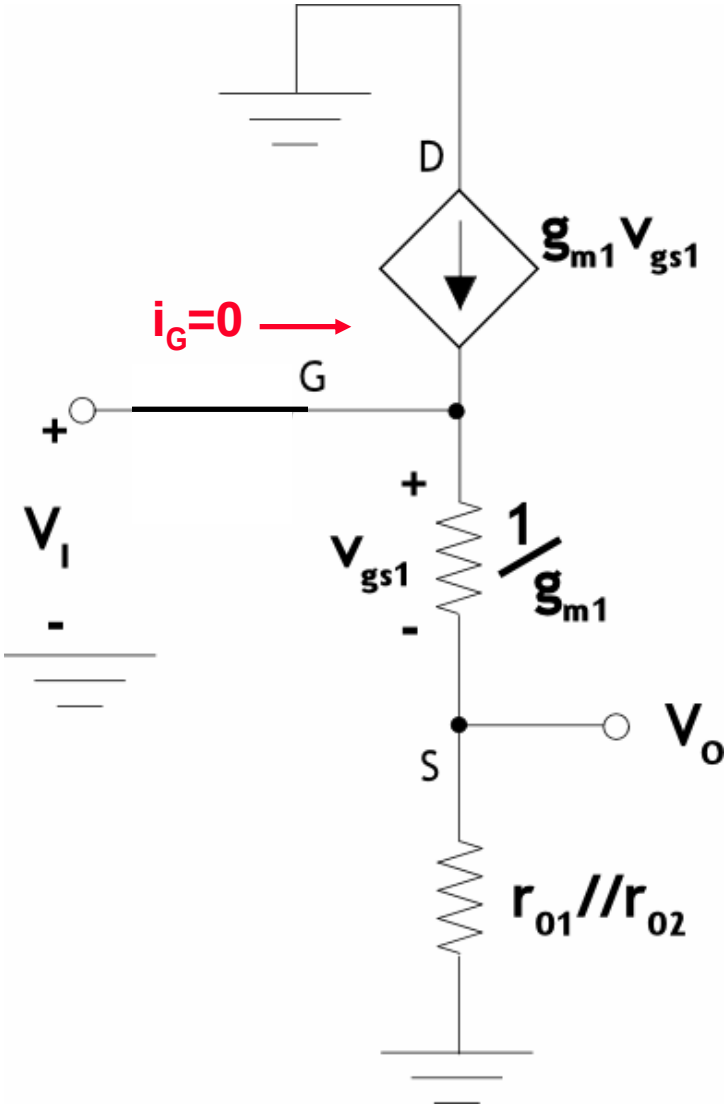
Two types of analysis:

Neglect AC Body-Effect

Use AC Body-Effect



CDA Without Body Effect

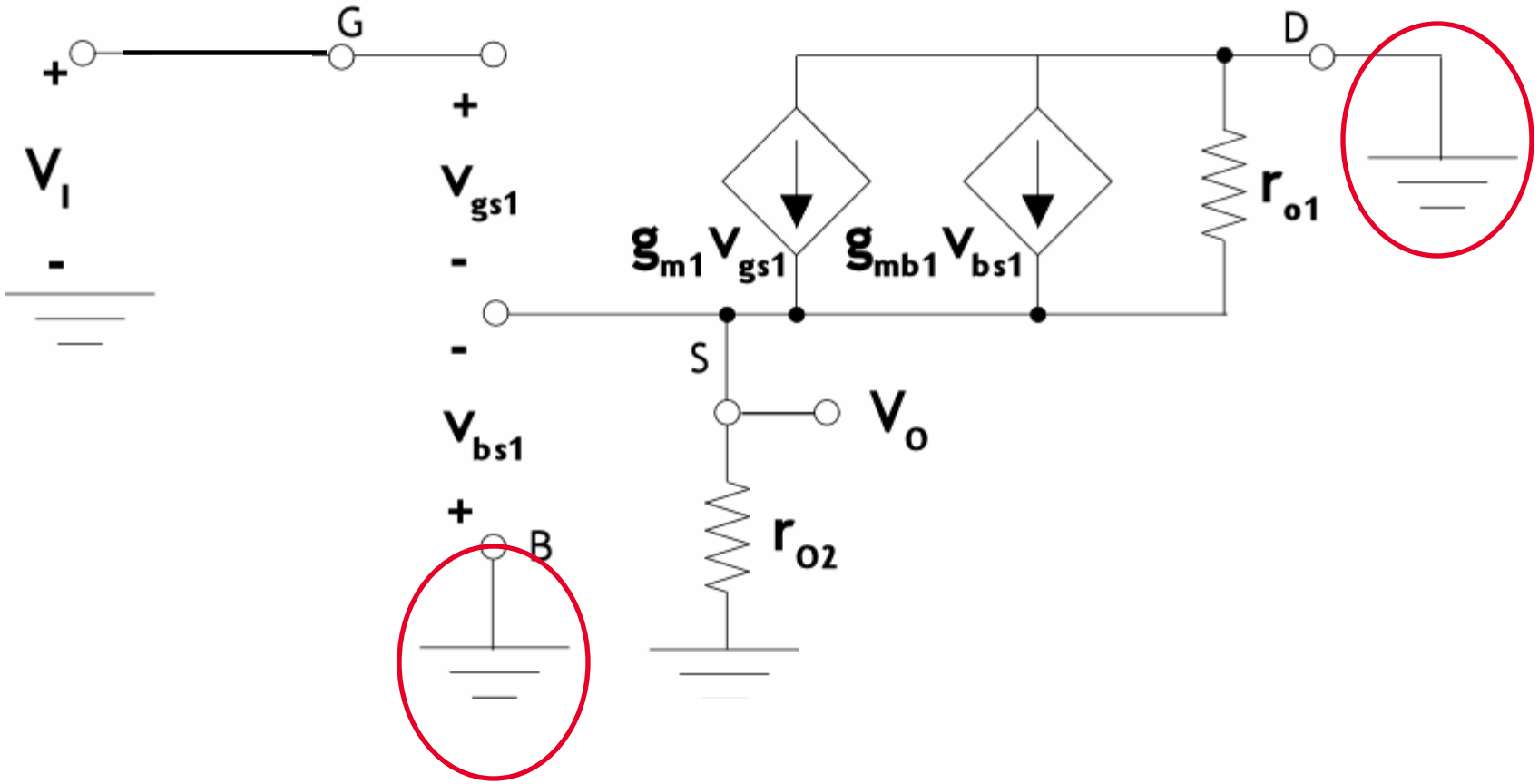


$$A_V = \frac{v_o}{v_I} = \frac{r_{o2}\|r_{o1}}{r_{o2}\|r_{o1} + \frac{1}{g_{m1}}}$$

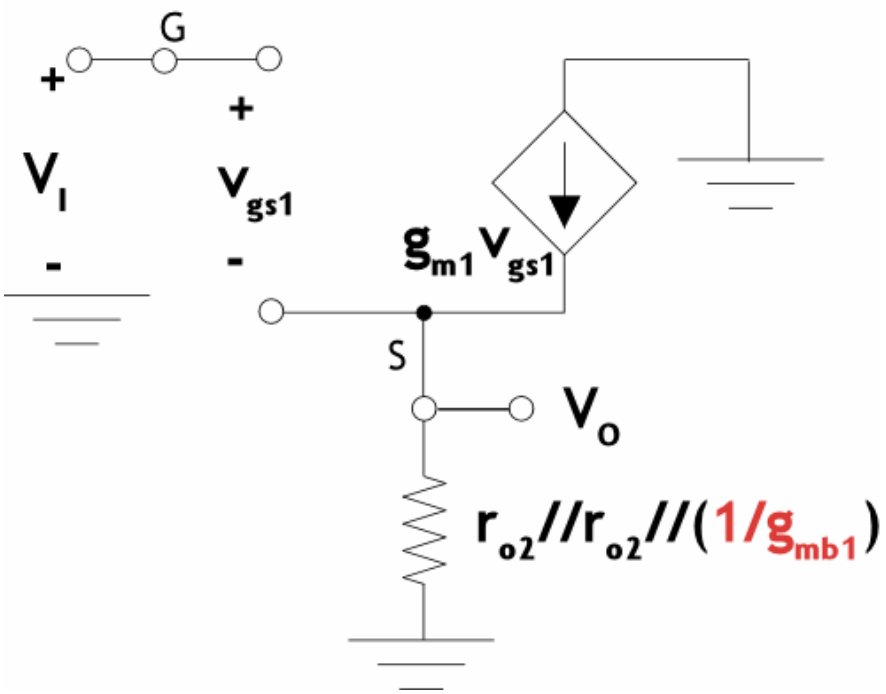
$$R_{IN} \Rightarrow \infty$$

$$R_{OUT} = r_{o1}\|r_{o2}\|\frac{1}{g_{m1}}$$

CDA With Body Effect



CDA With Body Effect



$$v_{gs1} = v_I - v_o$$

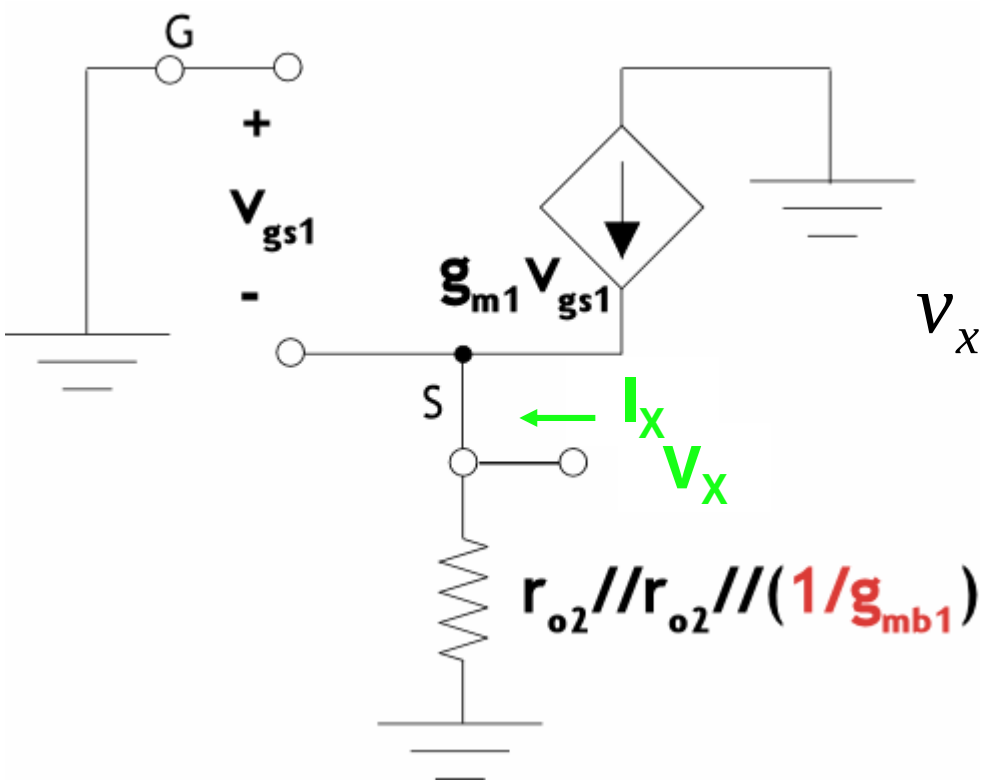
$$v_o = \left(g_{m1}v_{gs1}\right)\left(r_{o2}\|r_{o1}\|\frac{1}{g_{mb1}}\right)$$

$$= g_{m1}\left(v_I - v_o\right)\left(r_{o2}\|r_{o1}\|\frac{1}{g_{mb1}}\right)$$

$$\frac{v_o}{v_I} = \frac{\left(r_{o2}\|r_{o1}\|\frac{1}{g_{mb1}}\right)}{\left(r_{o2}\|r_{o1}\|\frac{1}{g_{mb1}}\right)+\frac{1}{g_{m1}}}$$

$$R_{IN} \Rightarrow \infty$$

CDA With Body Effect - R_{OUT}



Short input voltage source

$$v_{gs1} = -v_x$$

$$v_x = \left(g_{m1}v_{gs1} + i_x\right)\left(r_{o2}\left\|r_{o1}\right\|\frac{1}{g_{mb1}}\right)$$

$$R_{OUT} = \frac{v_x}{i_x} = \frac{r_{o2}\left\|r_{o1}\right\|\frac{1}{g_{mb1}}}{1+g_{m1}\left(r_{o2}\left\|r_{o1}\right\|\frac{1}{g_{mb1}}\right)}$$

By source-absorption:

$$R_{OUT} = r_{o1}\,//\,r_{o2}\,//(1/g_{m1})\,//(1/g_{mb1})$$

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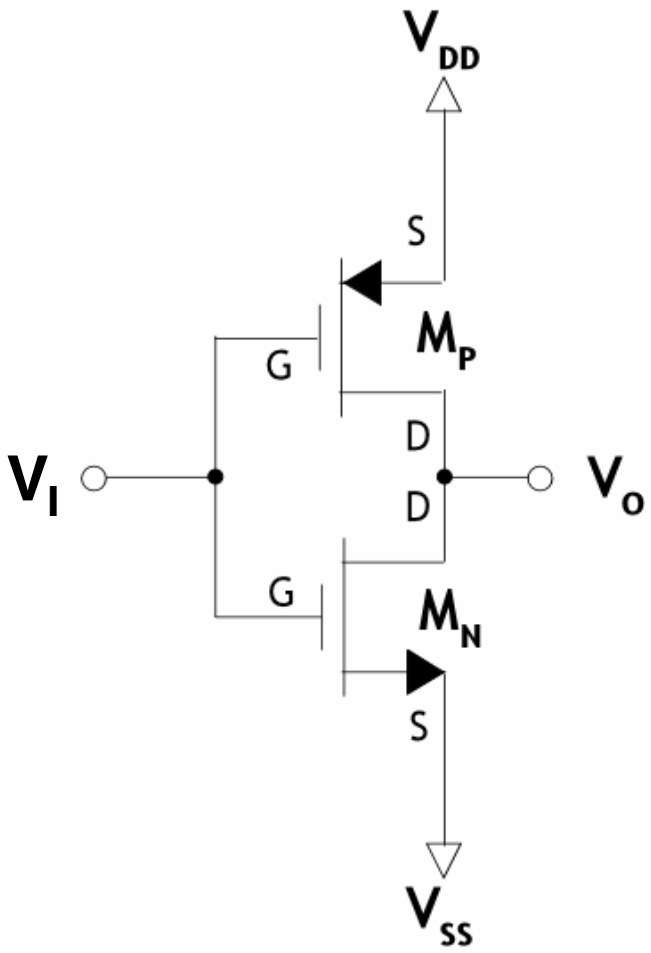
CMOS Inverter

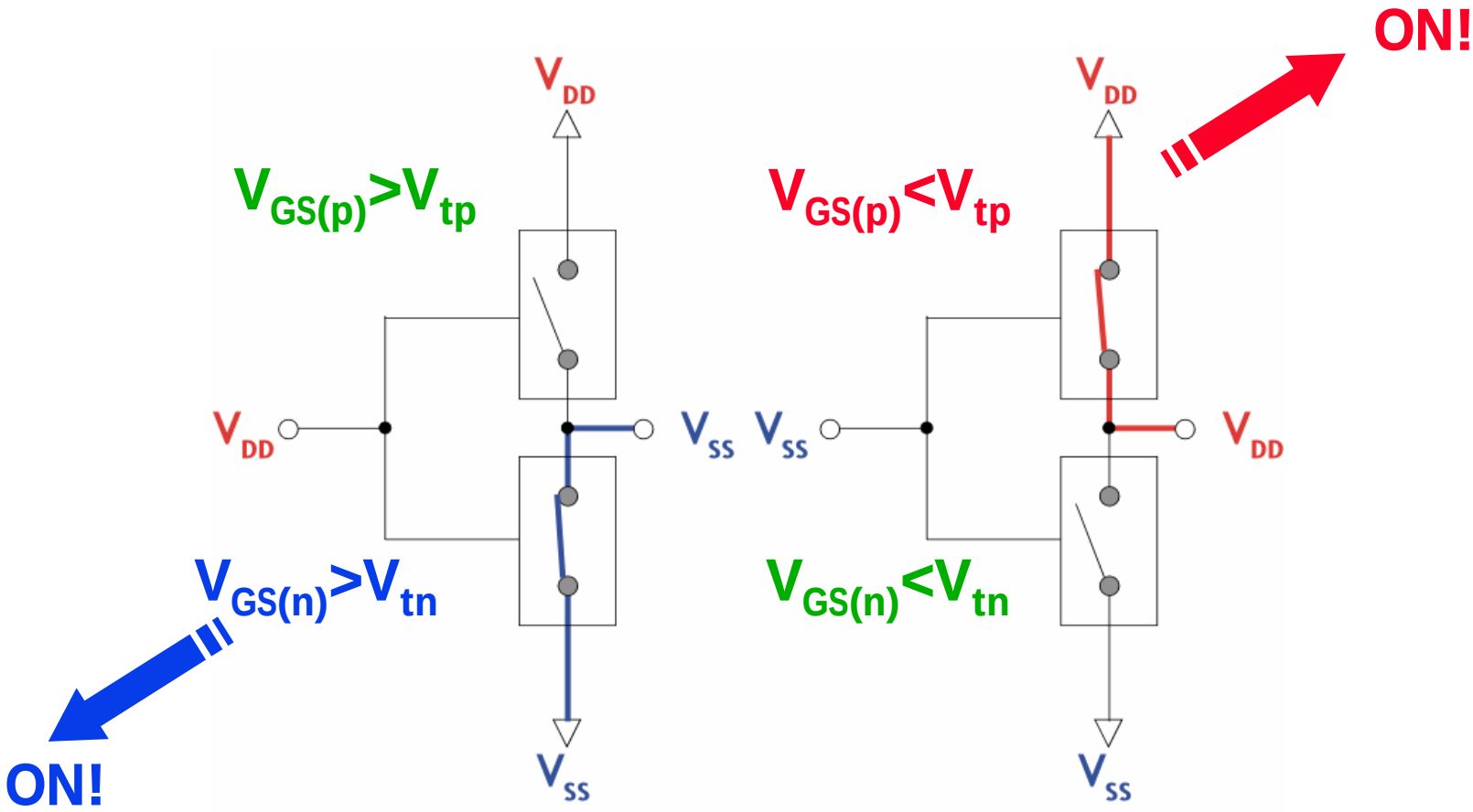


- MOSFETs can act as almost ideal current switches with symmetric VTCs.
- Matching of M_P and M_N: $|V_{tP}| = V_{tN} = V_t$
- Since typically k'_P is 2-3 times smaller than k'_n, the widths of the transistors are used to compensate:

$$W_P = 3W_N \quad \Longrightarrow \quad k'_p \frac{W_P}{L_P} = k'_n \frac{W_N}{L_N}$$

- This is definition of matched devices; equal current driving and sinking capabilities when charging & discharging capacitive loads

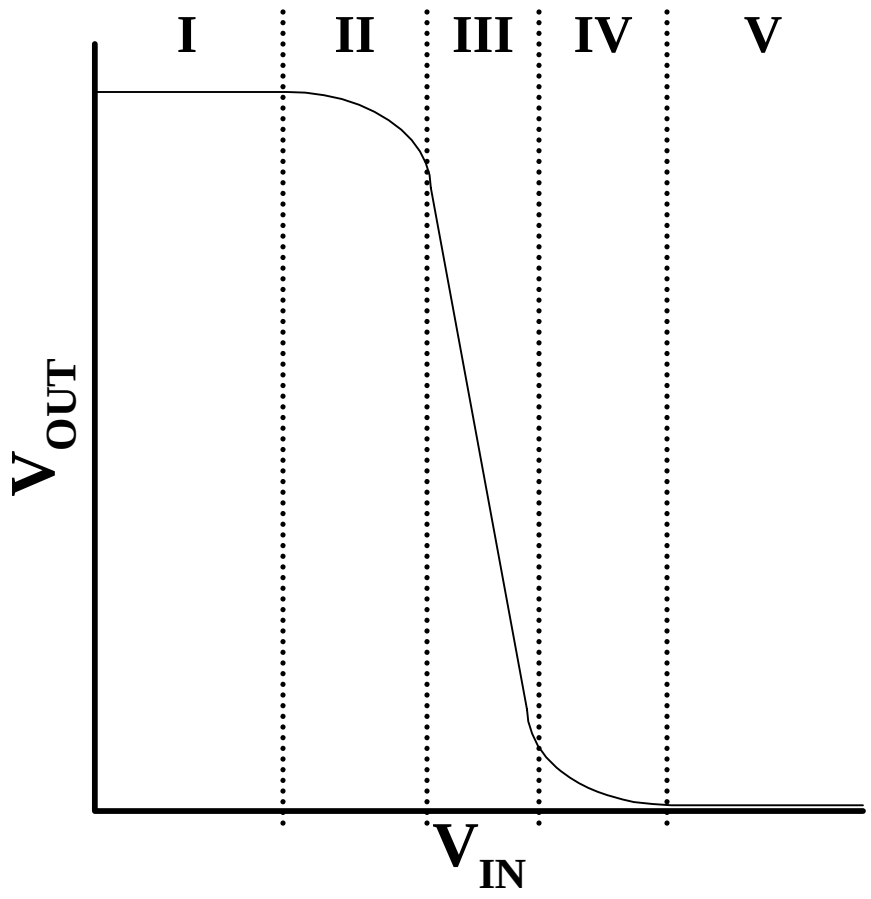
CMOS Inverter – Operation



nMOS transistor pulls output voltage to the most negative rail.

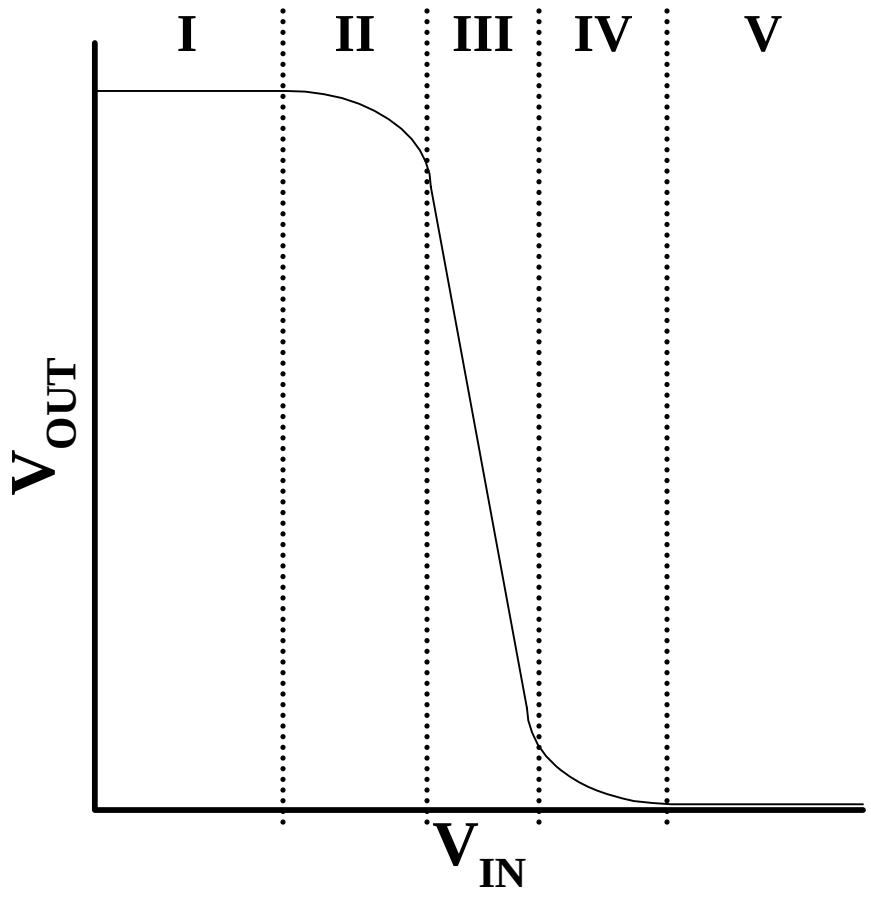
pMOS transistor pulls output voltage to the most positive rail.

Inverter VTC



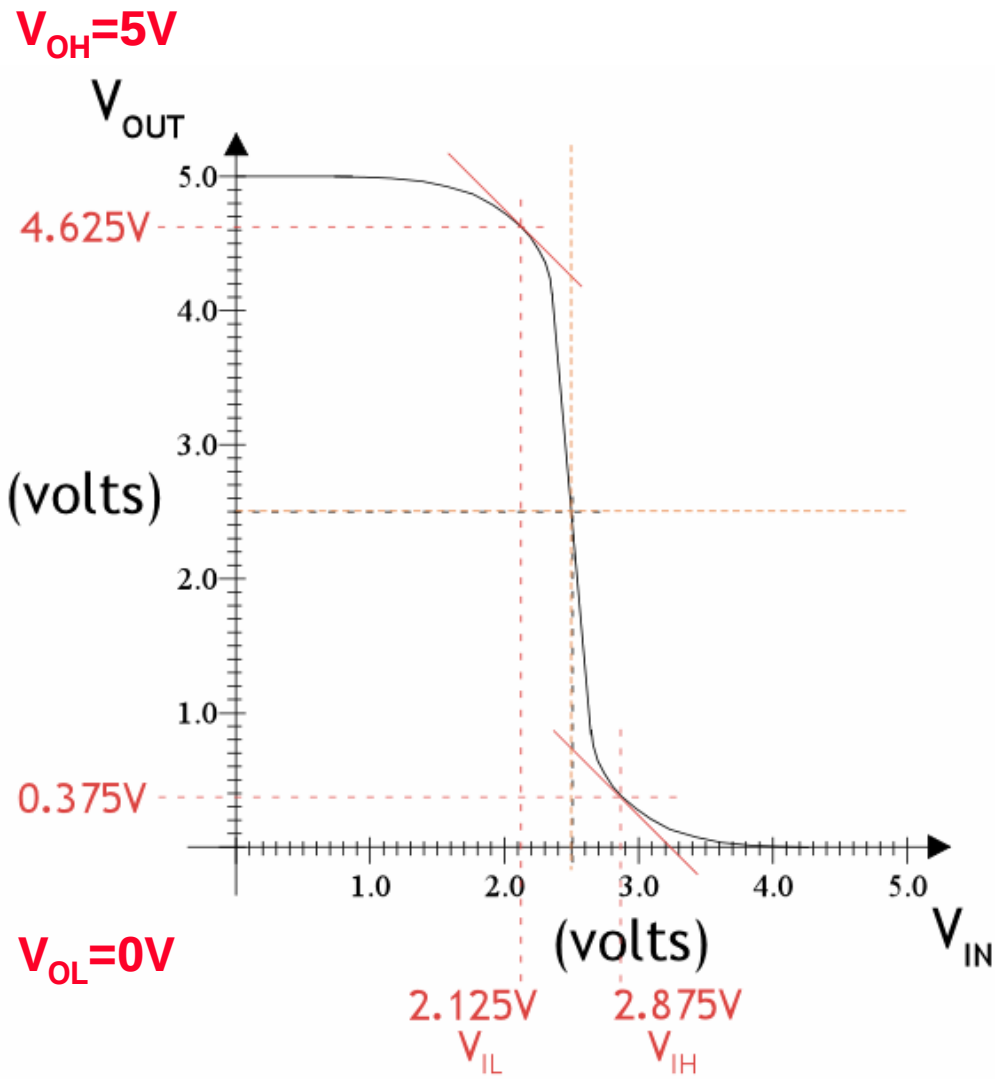
- Region I: $V_{IN} < V_t$
  - M_N cutoff, M_P in triode
  - Low-resistance path from V_{DD} to V_{OUT} pulls output high
  - No current flow
- Region II: $V_{IN} > V_t$
  - M_N enters saturation
  - M_P still in triode
  - Current flows, V_{OUT} starts to fall
- Region III:
  - High-gain region
  - M_N & M_P saturated
  - VTC slope = gain

Inverter VTC



- Region IV:
  - M_N enters triode
  - M_P still in saturation
- Region V: $V_{IN} > V_{DD}-V_t$
  - M_P cutoff, M_N in triode
  - Low-resistance path from V_{OUT} to ground pulls output low
  - No current flow

VTC Characteristics



- A matched inverter has symmetric voltage transfer characteristic.
- V_{OL} and V_{OH} are defined as 0V and 5V respectively.
- V_{IH} and V_{IL} defined as location where VTC slope = -1
  - V_{IL} is in region II
  - V_{IH} is in region IV

Finding V_{IH} – Matched Devices

- In region IV, M_P saturated, M_N in triode:

$$k_n'\frac{W_N}{L_N}\left[(V_{IN}-V_t)V_{OUT}-\frac{1}{2}V_{OUT}^2\right]=\frac{1}{2}k_n'\frac{W_P}{L_P}(V_{IN}-V_{DD}+V_t)^2$$

$$(V_{IN}-V_t)V_{OUT}-\frac{1}{2}V_{OUT}^2=\frac{1}{2}(V_{IN}-V_{DD}+V_t)^2 \quad (1)$$

- $V_{IN} = V_{IH}$ when $\frac{\partial V_{OUT}}{\partial V_{IN}}=-1$ $\therefore$ Take derivative wrt V_{IN}

$$V_{OUT}+(V_{IN}-V_t)\frac{\partial V_{OUT}}{\partial V_{IN}}-V_{OUT}\frac{\partial V_{OUT}}{\partial V_{IN}}=(V_{IN}-V_{DD}+V_t)$$

- Substitute $V_{IN} = V_{IH}$ & simplify to get: $V_{OUT}=V_{IH}-\frac{V_{DD}}{2}$

Finding V_{IH} – Matched Devices

- Take result for V_{OUT} when $V_{IN} = V_{IH}$

$$V_{OUT} = V_{IH} - \frac{V_{DD}}{2}$$

- Substitute into ①

$$(V_{IH} - V_t)\left(V_{IH} - \frac{V_{DD}}{2}\right) - \frac{1}{2}\left(V_{IH} - \frac{V_{DD}}{2}\right)^2 = \frac{1}{2}(V_{IH} - V_{DD} + V_t)^2$$

- Solving for V_{IH}, get: $V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)$

Finding V_{IL} – Matched Devices

- Can use similar procedure to find V_{IL}
  - Write equations for region II operation:M_P in triode, M_N in saturation
  - Solve for V_{OUT} when $V_{IN} = V_{IL}$ and substitute back into equations and solve for V_{IL}
- Result:

$$V_{IL} = \frac{1}{8}\left(3V_{DD} + 2V_t\right)$$

- Alternatively, can find V_{IL} using symmetry of VTC because V_{IL} and V_{IH} are symmetric about $V_{DD}/2$

$$V_{IH} - \frac{V_{DD}}{2} = \frac{V_{DD}}{2} - V_{IL}$$

Noise Margins

NM_H, High Noise Margin Definition:

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH} \qquad V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)$$

$$NM_H = V_{OH} - V_{IH} = \frac{1}{8}(3V_{DD} + 2V_t)$$

NM_L: Low Noise Margin Definition:

$$NM_L = V_{IL} - V_{OL} = V_{IL} - 0 \qquad V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t)$$

$$NM_L = V_{IL} - V_{OL} = \frac{1}{8}(3V_{DD} + 2V_t)$$

Conclusion: NMs equal for matched devices (Problem 4.107)

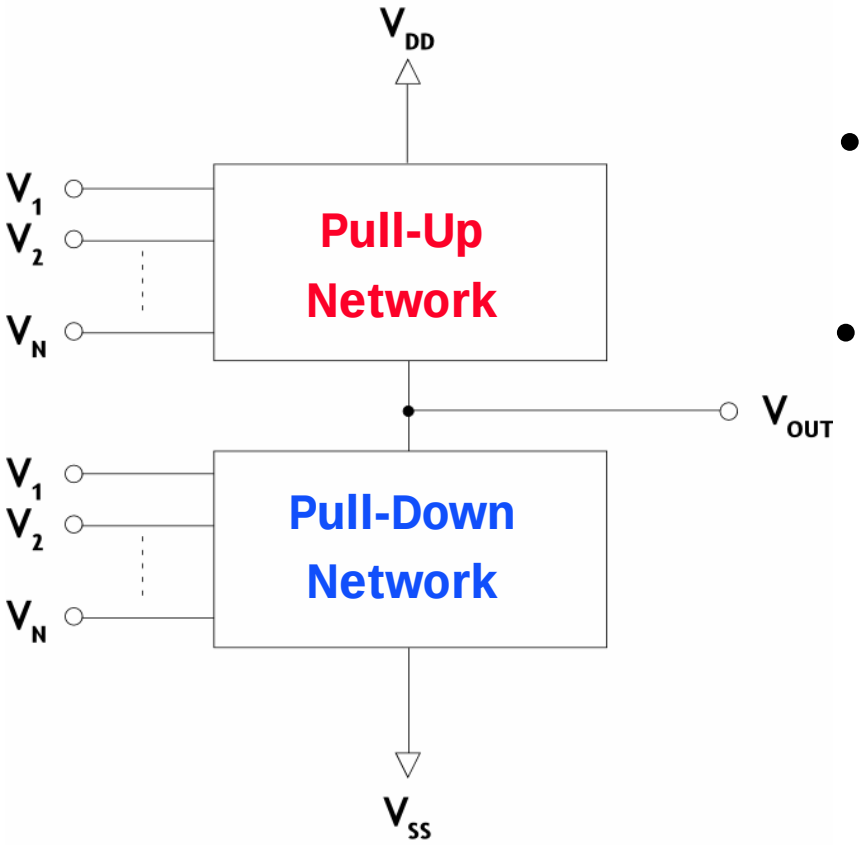
Mismatched Inverter Characteristics

- For mismatched devices:

$$\left|V_{tp}\right| \neq V_{tn} \qquad k'_p \frac{W_P}{L_P} \neq k'_n \frac{W_N}{L_N}$$

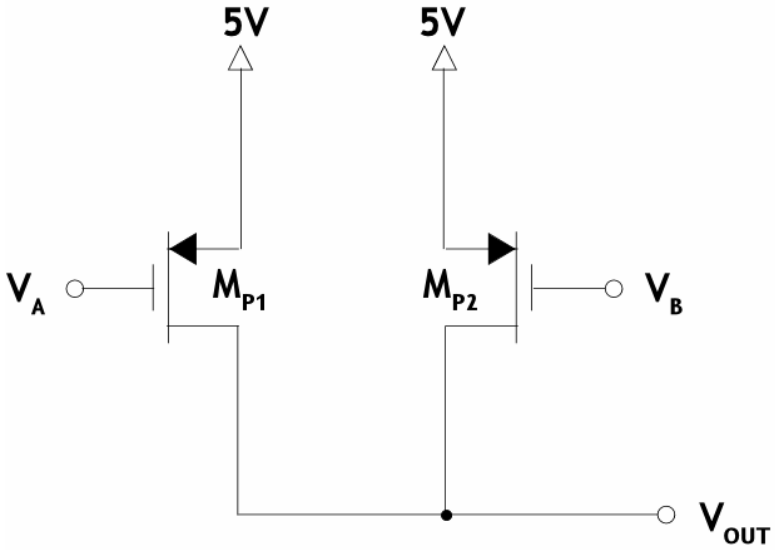
- VTC not symmetric any longer
- V_{IL} and V_{IH} can be found using same approach as before, with more algebra
- Resulting VTC noise margins will not be equal, but V_{OH} and V_{OL} will be unchanged

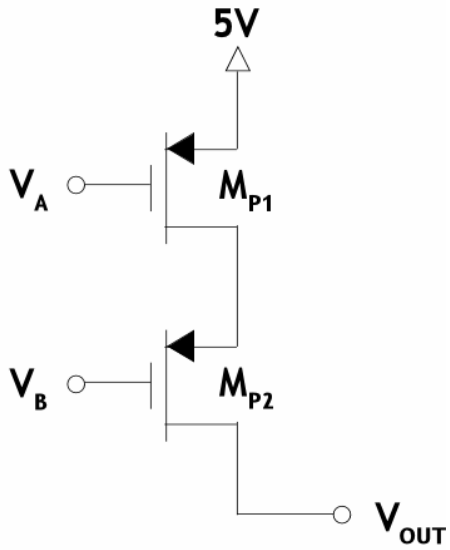
Structure of CMOS Logic-Gates



- **P-U-N: pull-up network** (PMOS transistors)
- **P-D-N: pull-down network** (NMOS transistors)
- P-U-N & P-D-N almost invariably made ***complementary*** networks
  - i.e. series-connected transistors in one network are parallel-connected in the other & vice versa
  - Facilitates formal design and logic synthesis techniques

Basic Pull-Up Structures





Parallel Structure

V_{OUT} is high when *either* V_A *or* V_B is low

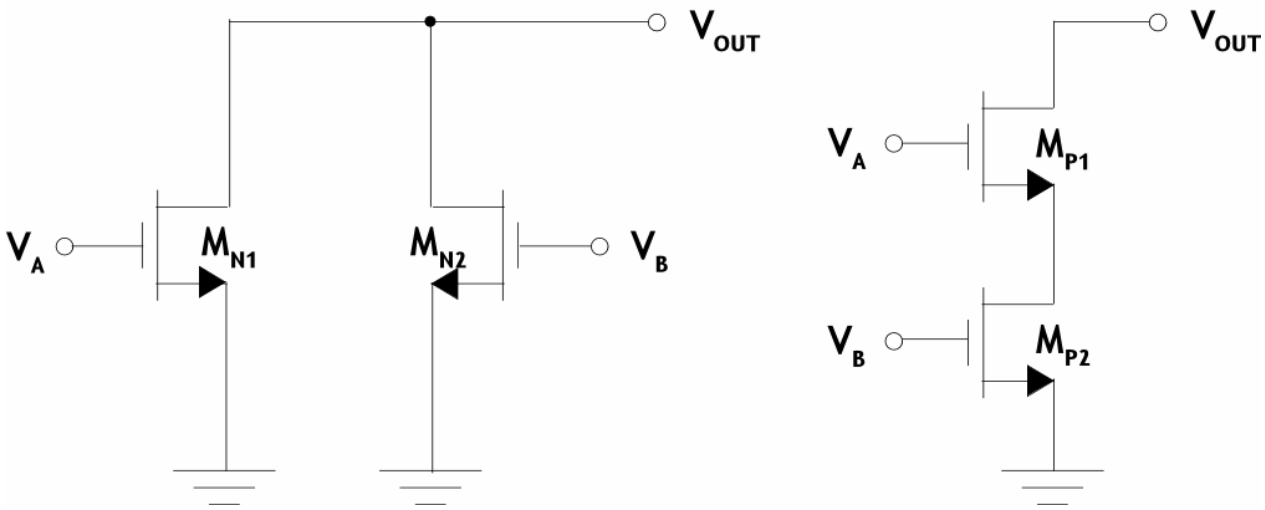
$$V_{OUT} = \overline{V_A} + \overline{V_B}$$

Serial Structure

V_{OUT} is high when *both* V_A *and* V_B are low

$$V_{OUT} = \overline{V_A} \cdot \overline{V_B}$$

Basic Pull-Down Structures



Parallel Structure

V_{OUT} is low when *either* V_A *or* V_B is high

$$\overline{V_{OUT}} = V_A + V_B$$

Serial Structure

V_{OUT} is low when *both* V_A *and* V_B are high

$$\overline{V_{OUT}} = V_A \cdot V_B$$

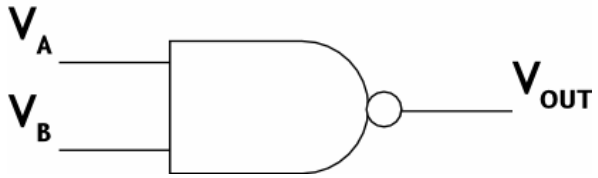
2-Input CMOS NAND Gate

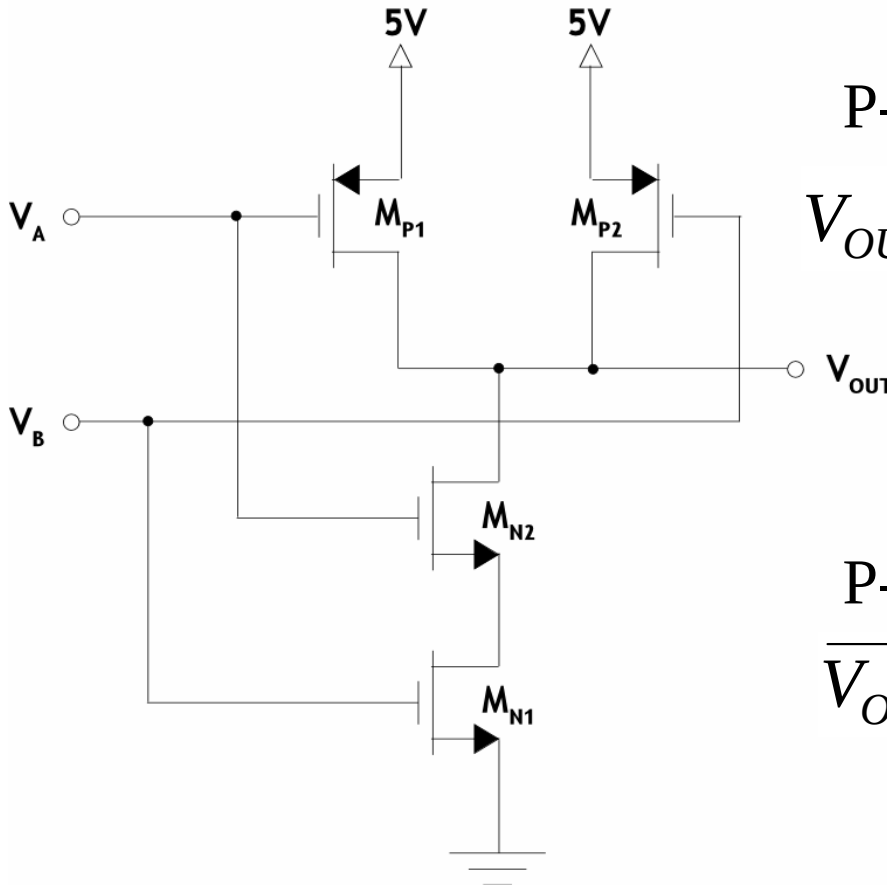
Truth table:

V_A	V_B	V_{OUT}
0	0	1
1	0	1
0	1	1
1	1	0

$$V_{OUT} = \overline{V_A \cdot V_B}$$

Logic Symbol:





P-U-N:

$$V_{OUT} = \overline{V_A} + \overline{V_B}$$

P-D-N:

$$\overline{V_{OUT}} = V_A \cdot V_B$$

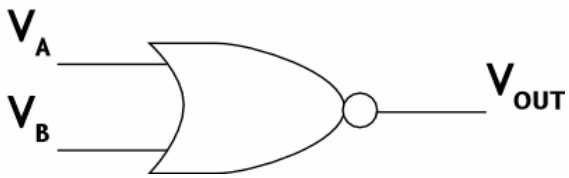
2-Input CMOS NOR Gate

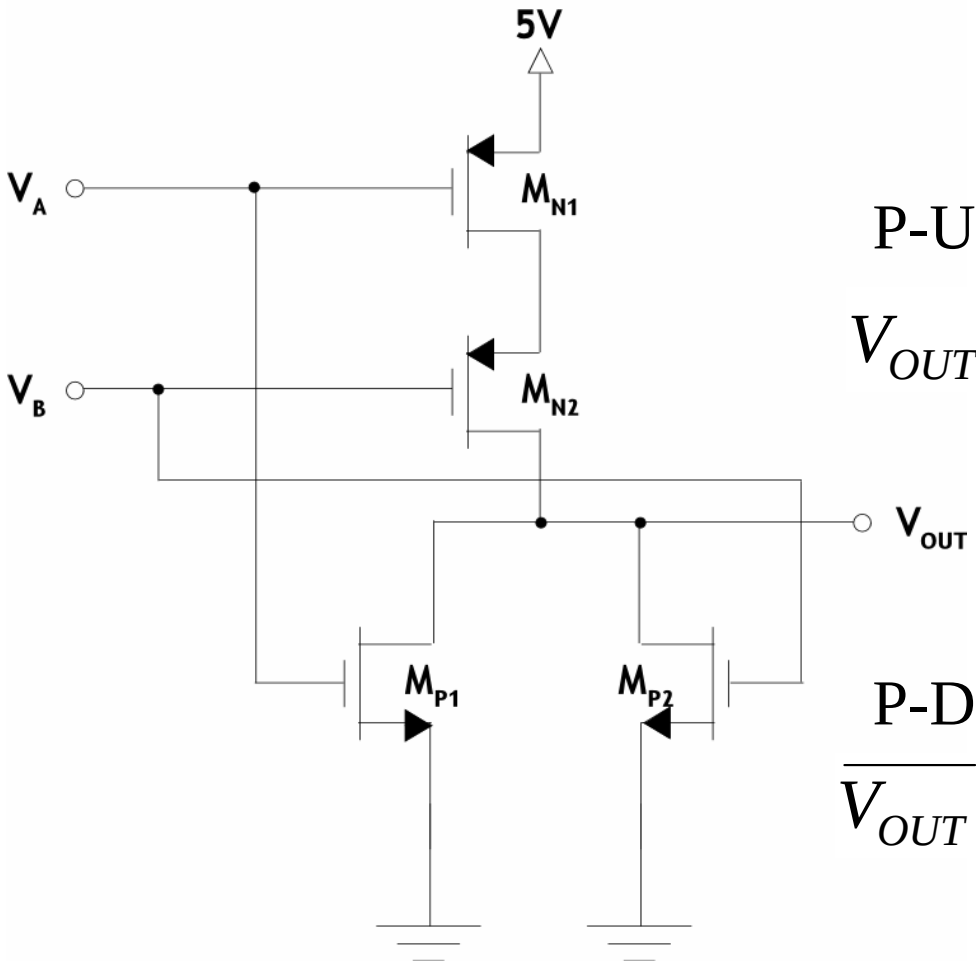
Truth table:

V_A	V_B	V_{OUT}
0	0	1
1	0	0
0	1	0
1	1	0

$$V_{OUT} = \overline{V_A + V_B}$$

Logic Symbol:





P-U-N:

$$V_{OUT} = \overline{V_A} \cdot \overline{V_B}$$

P-D-N:

$$\overline{V_{OUT}} = V_A + V_B$$

Outline of Chapter 4, Sections 4.8-4.9

- 1- High-Frequency Model of MOSFET
- 2- Frequency Response of CSA
- Note: Frequency response of CGA and CDA are covered in EC2

High-Frequency Model

- The small signal model discussed so far didn't include internal capacitances and resulted in constant gain without accounting for frequency changes.
- Internal capacitances:
  - The gate capacitive (Cox) effect is modeled by three capacitors Cgs, Cgd and Cgb
  - The source-body and drain-body depletion layer capacitances: Reverse biased pn junctions

Gate Capacitive Effect

- In Triode region the channel has a uniform depth:

$$C_{gs} = C_{gd} = \frac{1}{2} WLC_{ox}$$

- In saturation region: Channel is pinched off:

$$C_{gs} = \frac{2}{3} WLC_{ox} \qquad C_{gd} = 0$$

- In the cutoff region: $C_{gs} = C_{gd} = 0$
- Often there is overlap area underneath the gate in the S and D diffusion (n^+ or P^+) regions.
  - This adds to Cgs and Cgd

Junction Capacitances

- The two pn junction in MOSFET are reverse biased, so the depletion regions creates junction capacitances
- Junction capacitance in a reverse-biased diode or pn junction is defined by:

$$C_j = \frac{C_{j0}}{\left(1+\frac{V_R}{V_0}\right)^m} \qquad \frac{1}{3} \le m \le \frac{1}{2} \qquad C_j = \frac{C_{j0}}{\sqrt{1+\frac{V_R}{V_0}}}$$

- Where V0 is the junction built-in voltage, Cj0 is the value of Cj when zero voltage is applied and m is the grading coefficient

Junction Capacitances

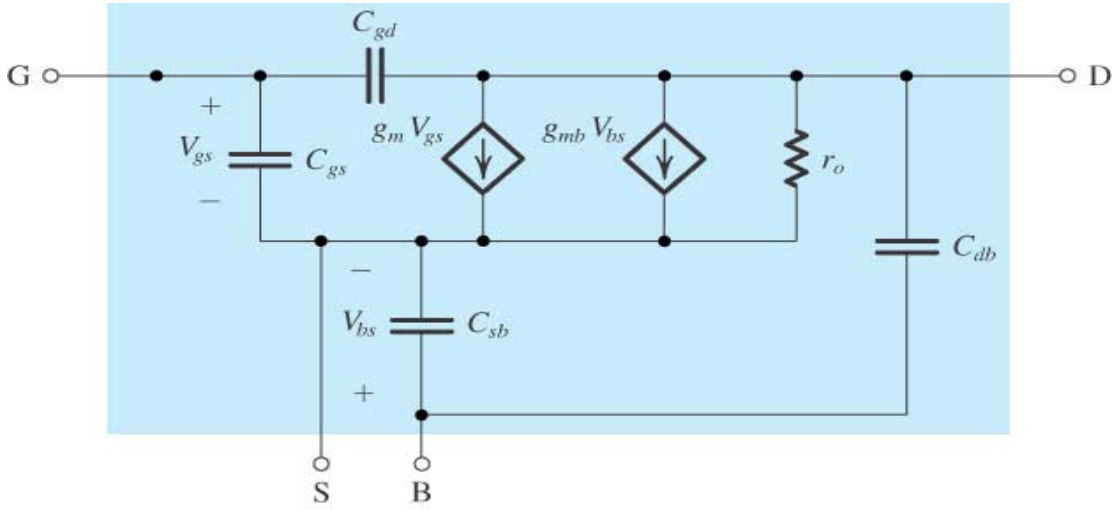
- The two junction capacitances in MOSFET are:

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1+\frac{V_{SB}}{V_0}}} \qquad C_{db} = \frac{C_{db0}}{\sqrt{1+\frac{V_{DB}}{V_0}}}$$

- Assuming m=1/2
- V0 is the junction built-in voltage (0.6 to 0.8 V)
- Csb0 is the value of Csb at VSB=0
- Cdb0 is the value of Cdb at VDB=0
- Formulas are for small-signal operation

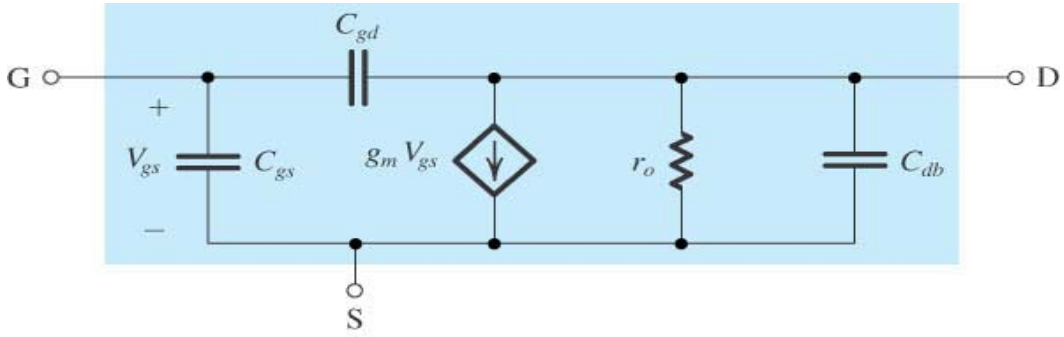
High-Frequency MOSFET Model

- Complete Model used in SPICE (Fig. 4.47):



(a)

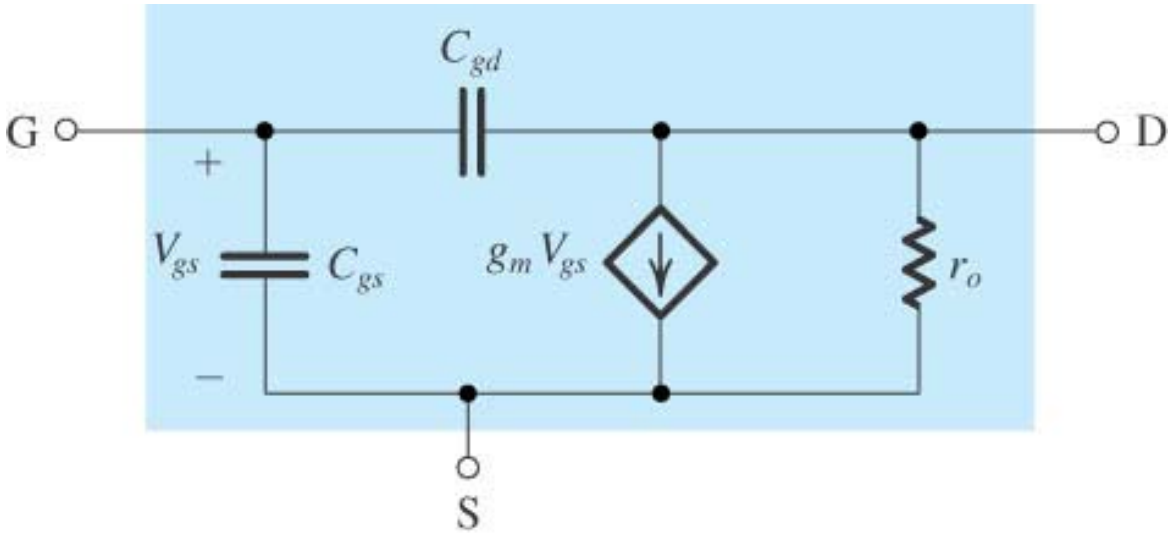
- When S is connected to B:



(b)

High-Frequency MOSFET Model

- Capacitance C_{db} is usually neglected and for hand calculations and circuit solutions the following model is used

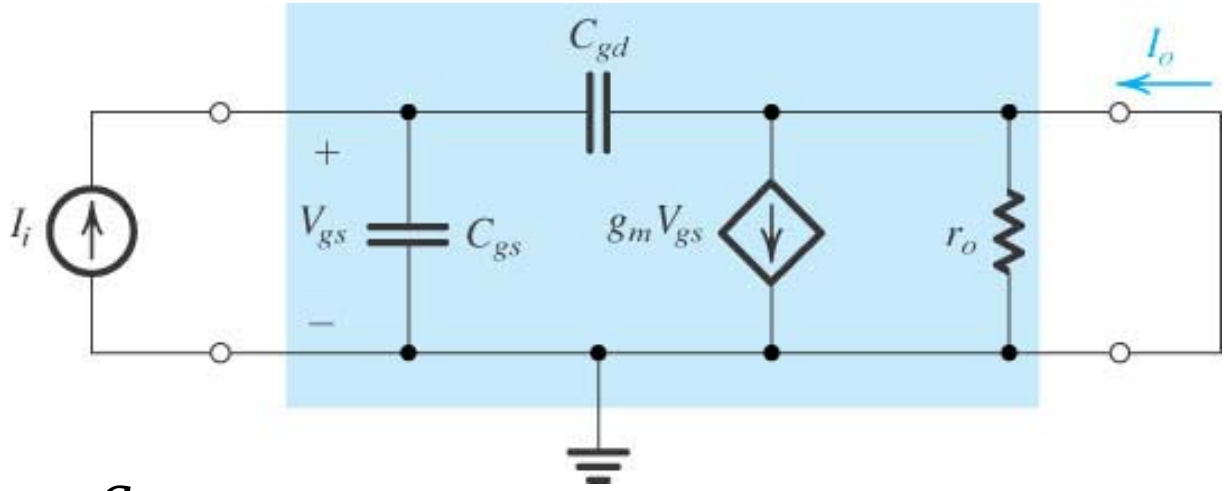


(c)

- Note: Hybrid-π model is used

MOSFET Unity-Gain Frequency

- Unity-gain frequency, f_T, is a figure of merit for high-frequency operation.
- It is defined as the frequency at which the short circuit current gain in the Common Source amplifier is 1.



$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

Goes up to few GHz

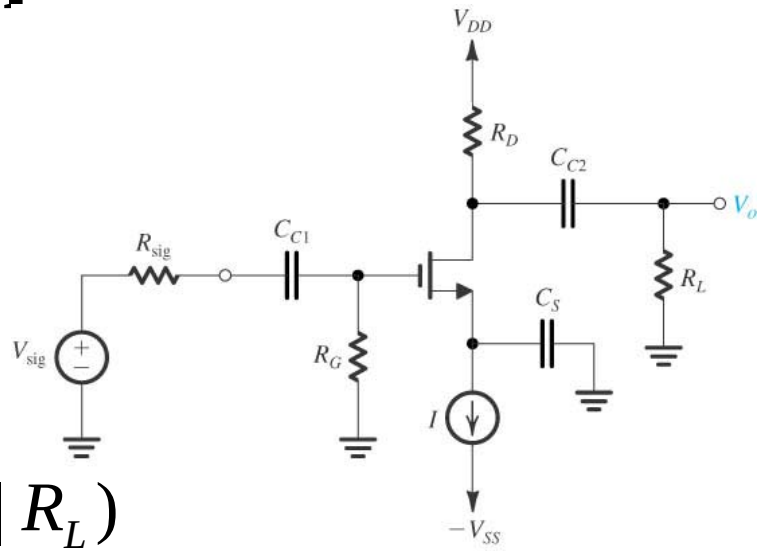
Frequency Response of CSA

- Gain expressions derived previously were assumed to be independent of frequency.
- In reality gain is constant only over the midband frequencies
- The midband gains are the gain relations we found earlier
- Low frequency falloff is due to coupling and bypass capacitors
- High frequency gain falloff is due to internal capacitances.

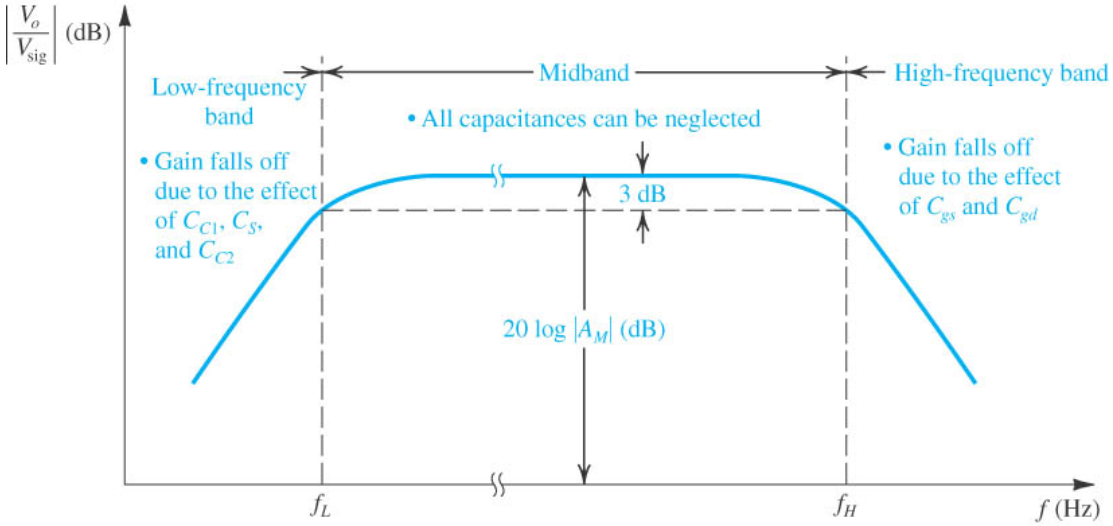
Frequency Response of CSA

- Midband gain:

$$A_M = \frac{V_o}{V_{sig}} = -\frac{R_G}{R_G + R_{sig}} g_m (r_o \parallel R_D \parallel R_L)$$



(a)



(b)

High-Frequency Response (CSA)

- f_H and f_L are frequencies at which gain is 3 dB lower than the midband value
- 3dB bandwidth is:

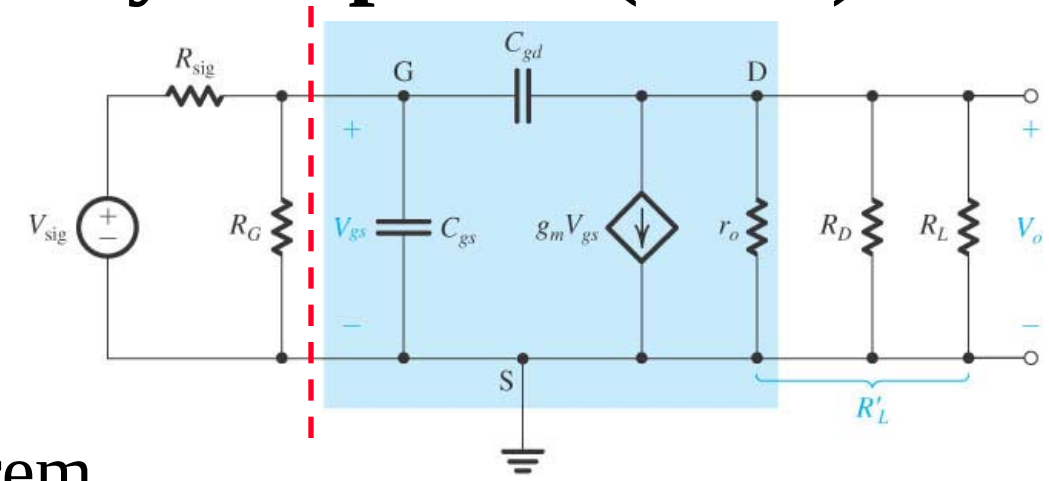
$$BW \equiv f_H - f_L$$

- If $f_L << f_H$ then $$BW \cong f_H$$
- Another figure of merit for an amplifier is gain-bandwidth product

$$GB \equiv |A_M| BW$$

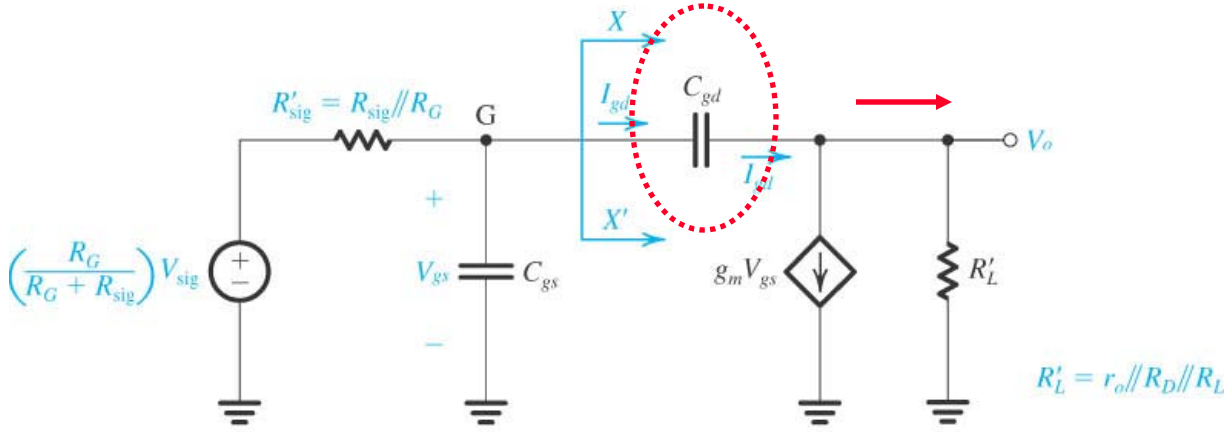
High-Frequency Response (CSA)

- CSA



(a)

- Using Thevenin Theorem

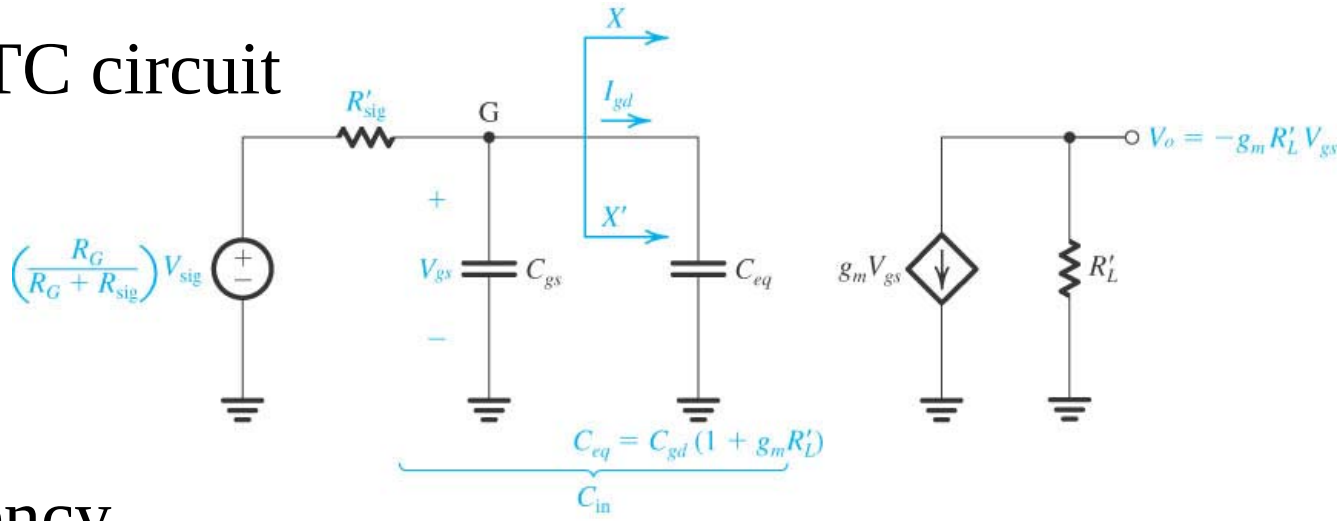


(b)

High-Frequency Response (CSA)

- Lowpass STC circuit

Miller Effect



- Corner frequency

$$\omega_H = \omega_0 = \frac{1}{C_{in} R'_{sig}} = \frac{1}{(C_{gs} + C_{eq}) R'_{sig}}$$

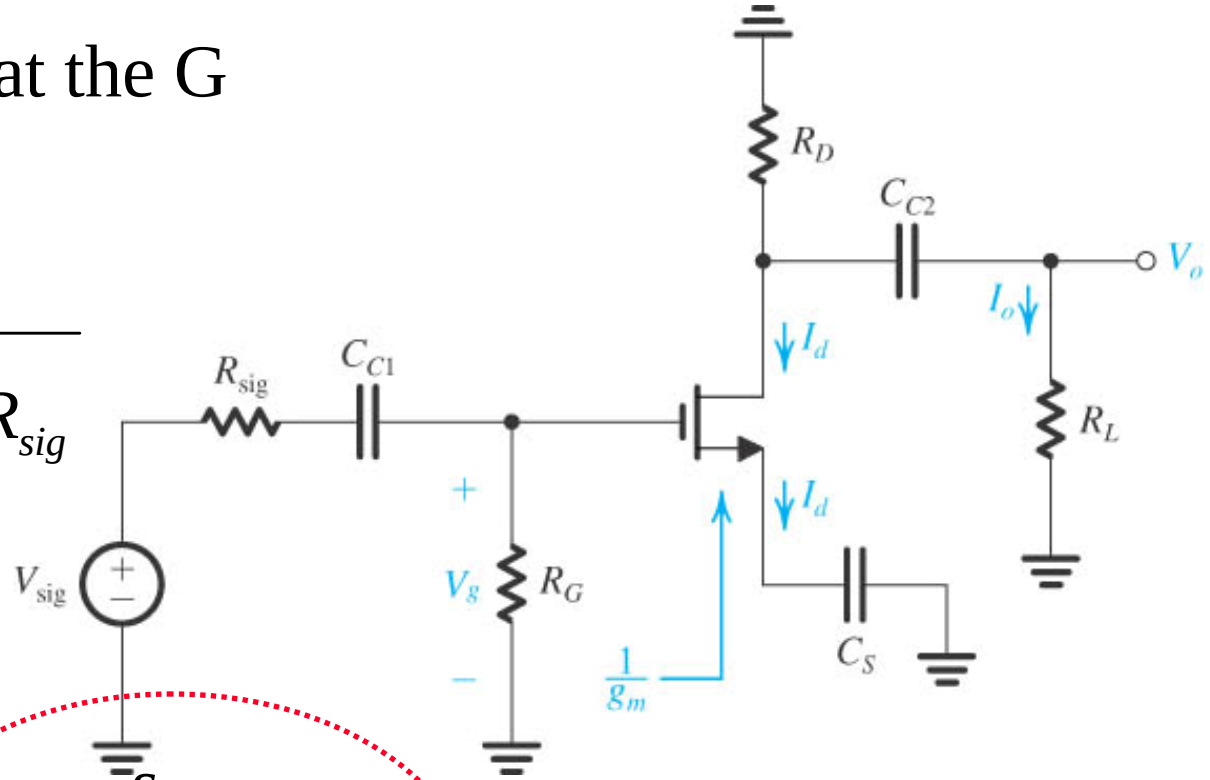
- High-frequency gain of CSA

$$\frac{V_o}{V_{sig}} = \frac{A_M}{1 + \frac{s}{\omega_H}} = -\frac{R_G}{R_G + R_{sig}} (g_m R'_L) \frac{1}{1 + \frac{s}{\omega_H}}$$

Low-Frequency Response (CSA)

- Voltage divider at the G

$$V_g = V_{sig}\frac{R_G}{R_G + \dfrac{1}{sC_{C1}} + R_{sig}}$$



$$V_g = V_{sig}\frac{R_G}{R_G + R_{sig}}\cdot\frac{s}{s + \dfrac{1}{C_{C1}(R_G + R_{sig})}}$$

High-pass STC

$\omega_0 = \omega_{p1}$

Low-Frequency Response (CSA)

- Two other high-pass factors are due to:
  - Source bypass capacitance $\omega_{p2} = \frac{g_m}{C_S}$
  - Load coupling capacitance $\omega_{p3} = \frac{1}{C_{C2}(R_D + R_L)}$
- Low-frequency transfer function or low-frequency gain of CSA

$$\frac{V_o}{V_{sig}} = -\frac{R_G}{R_G + R_{sig}}(g_m R_D \| R_L)\frac{s}{s+\omega_{P1}}\frac{s}{s+\omega_{P2}}\frac{s}{s+\omega_{P3}}$$

Low-Frequency Response (CSA)

- To find the time constant for poles f_{p1}, f_{p2} and f_{p3}
  - Set source to zero
  - Consider each C separately (others are short circuit)
  - Find the total resistance seen between the two terminals of C